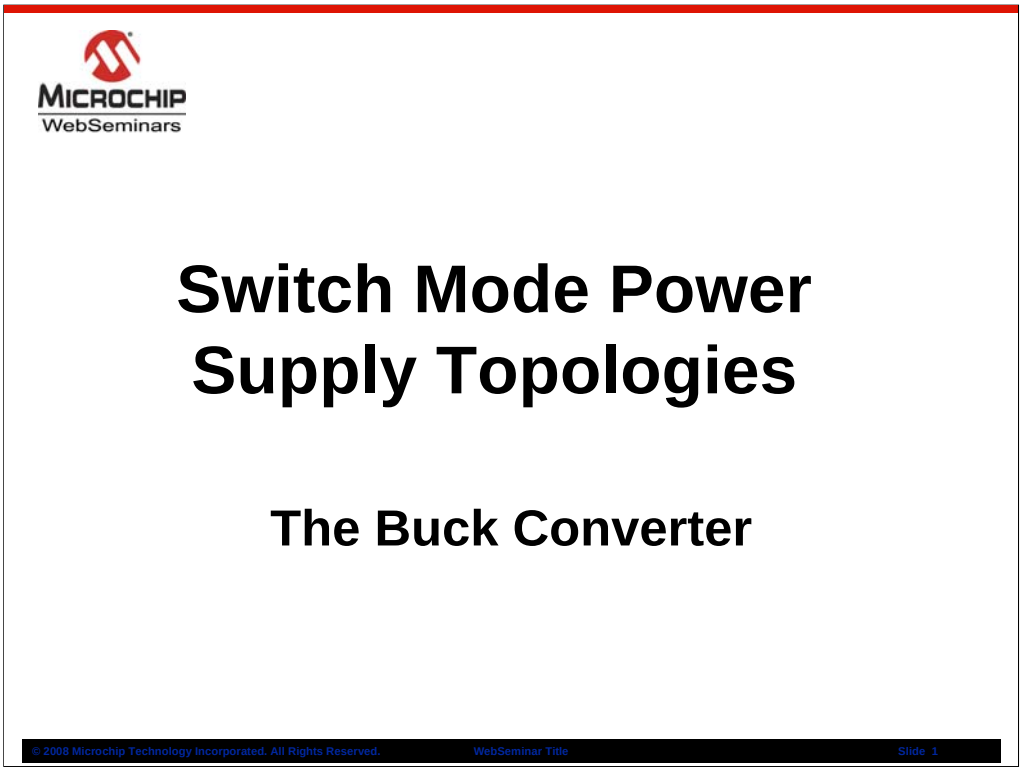
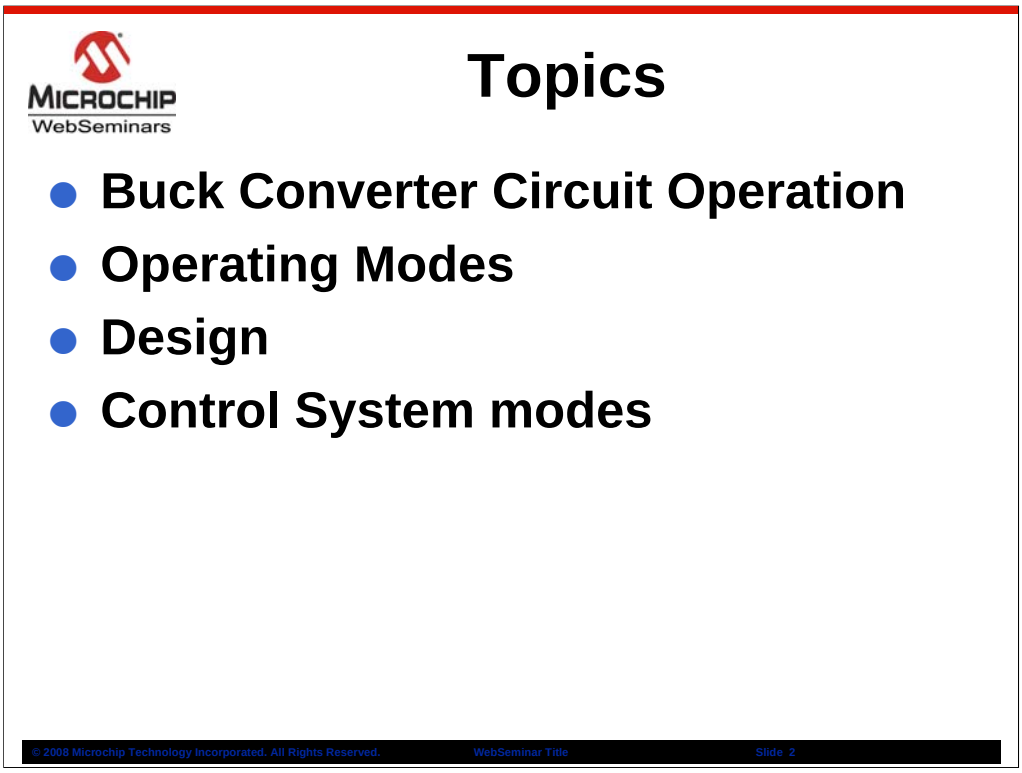
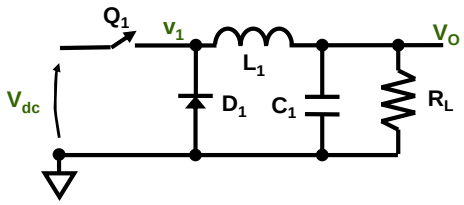


Welcome to this Web seminar on Switch Mode Power Supply Topologies. In this webinar, we will analyze the Buck Converter topology. The buck converter converts a higher input voltage to a lower output voltage. A similar function is also performed by a linear regulator. The most important difference then between the linear and switching approach is that the switching approach allows for a much higher efficiency.



We will start by discussing the basic operation of the buck converter circuit and it operating modes. We will then look at how the individual components of a the buck converter are designed. We conclude by taking a brief look at the available control system modes while using the buck converter.

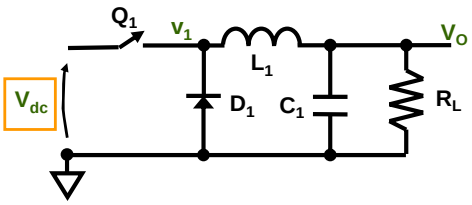
Buck Converter



- V_{dc} – Input DC Voltage
- V_o – Output DC Voltage
- Q_1 – Solid State switch operating at Frequency FPWM
- V_1 – Pulse Width Modulated Signal

This is a basic buck converter circuit.

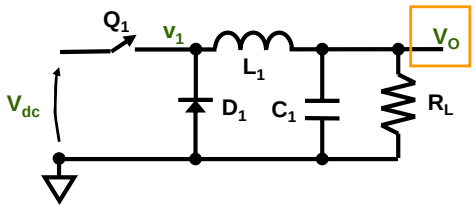
Buck Converter



- V_{dc} – Input DC Voltage
- V_o – Output DC Voltage
- Q_1 – Solid State switch operating at Frequency FPWM
- V_1 – Pulse Width Modulated Signal

The input to this circuit is a DC voltage V_{dc}

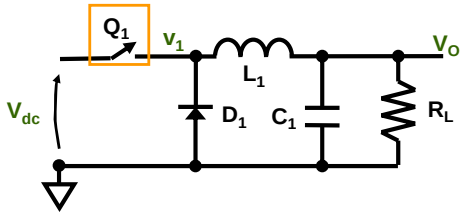
Buck Converter



- V_{dc} – Input DC Voltage
- V_o – Output DC Voltage
- Q_1 – Solid State switch operating at Frequency FPWM
- V_1 – Pulse Width Modulated Signal

and the output volatge is a DC voltage V_o.

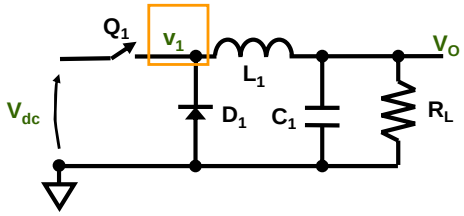
Buck Converter



- V_{dc} – Input DC Voltage
- V_o – Output DC Voltage
- Q_1 – Solid State switch operating at Frequency FPWM
- V_1 – Pulse Width Modulated Signal

Switch Q_1 is a solid state switch which opens and closes at a frequency F_{PWM}.

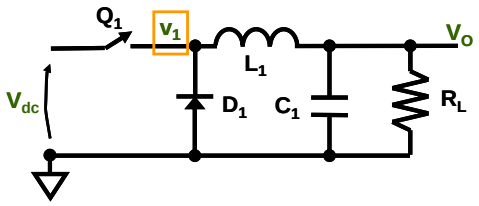
Buck Converter



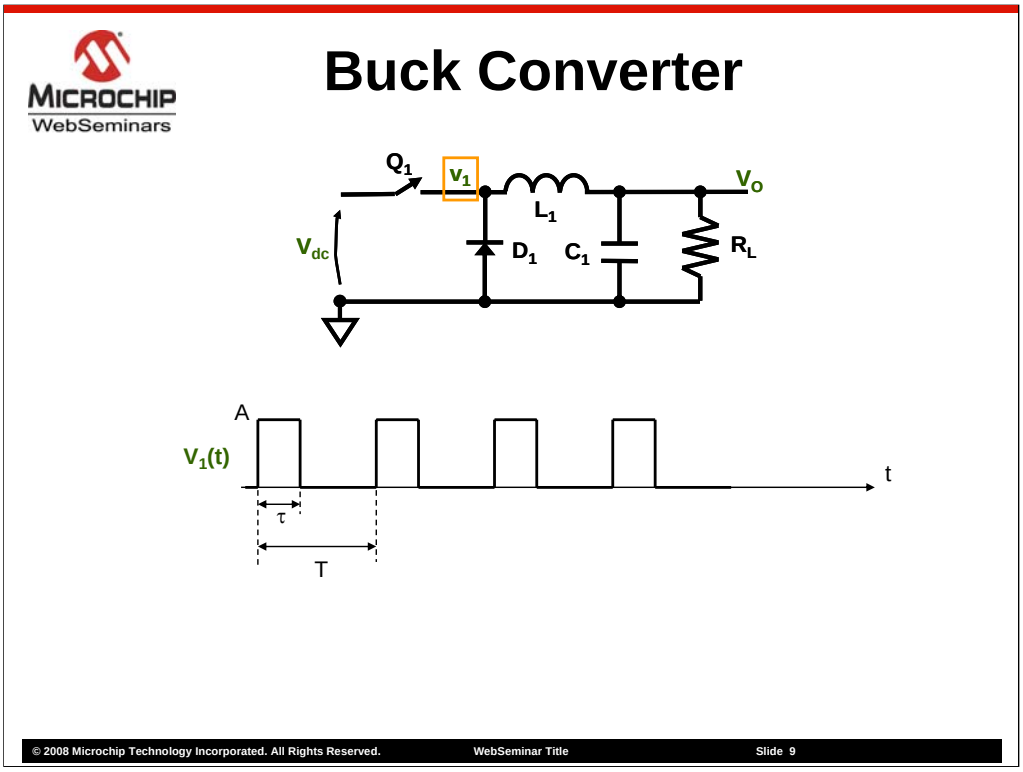
- V_{dc} – Input DC Voltage
- V_o – Output DC Voltage
- Q_1 – Solid State switch operating at Frequency FPWM
- V_1 – Pulse Width Modulated Signal

The opening and closing of switch Q_1 causes volatge V_1 to be a switched waveform with a ON time period and an off time period . During the ON time period V_1 is connected to V_{dc}. During the off time period V_1 is disconnected from V_{dc}. Volatge V_1 now becomes a pulse width modulated signal with a duty cycle dependant on the rate at which switch is operated. The amplitude of voltage V_o is then proportional to the duty cycle of voltage V_1.

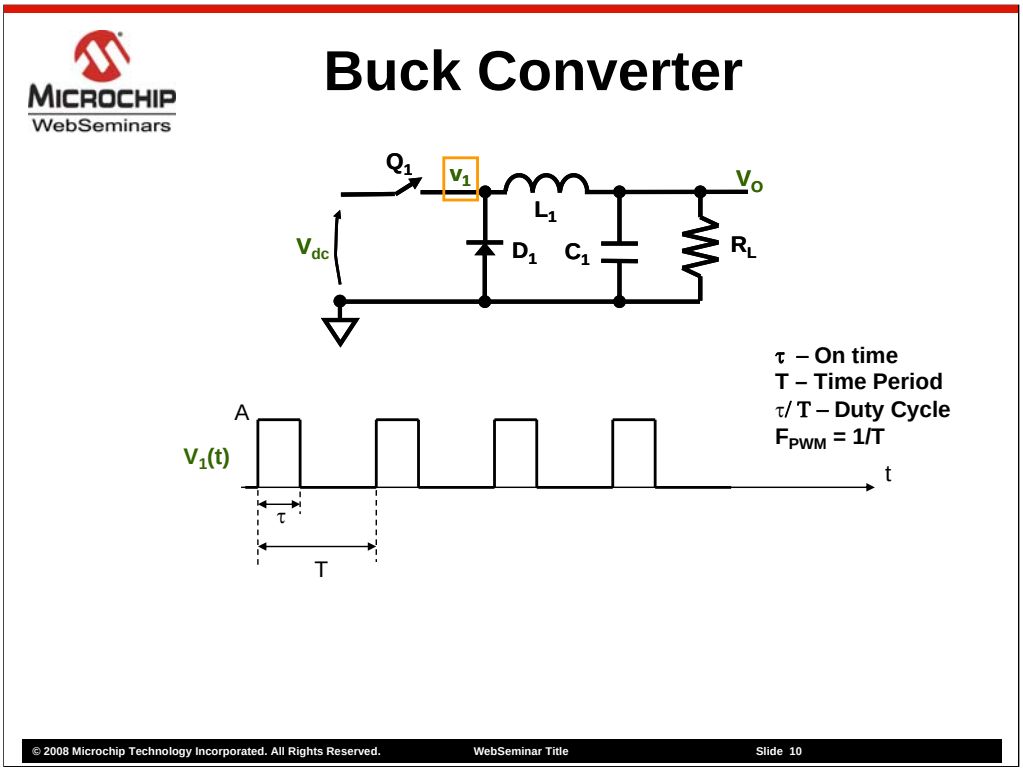
Buck Converter



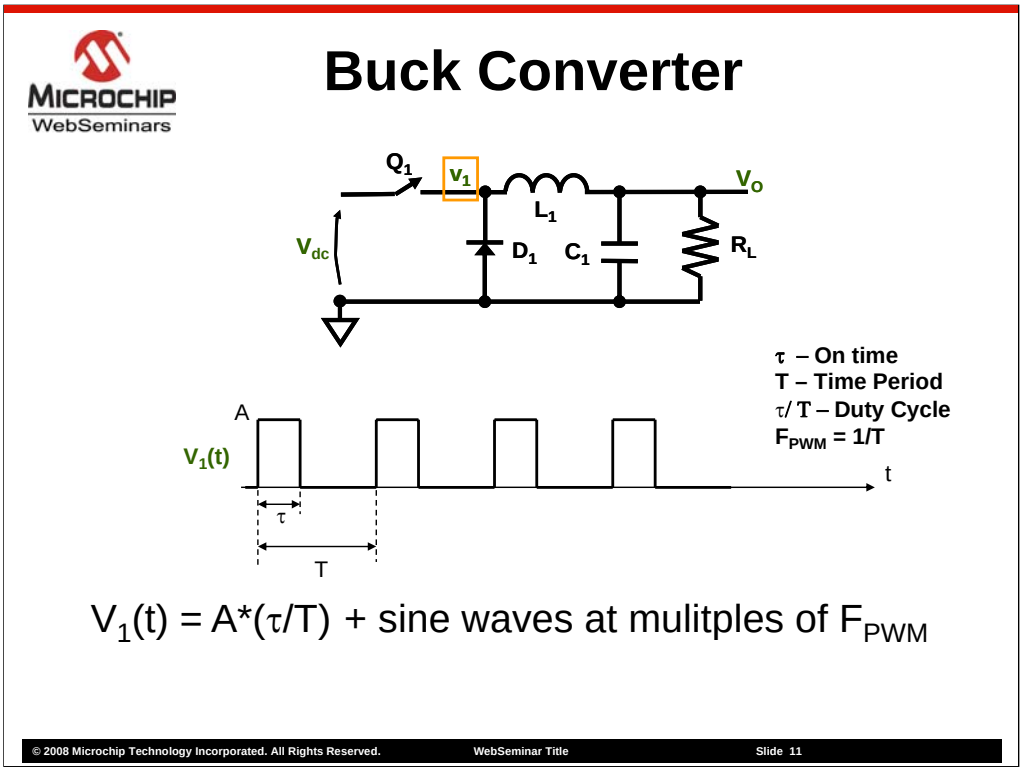
Lets analyze the switching waveform V_1.



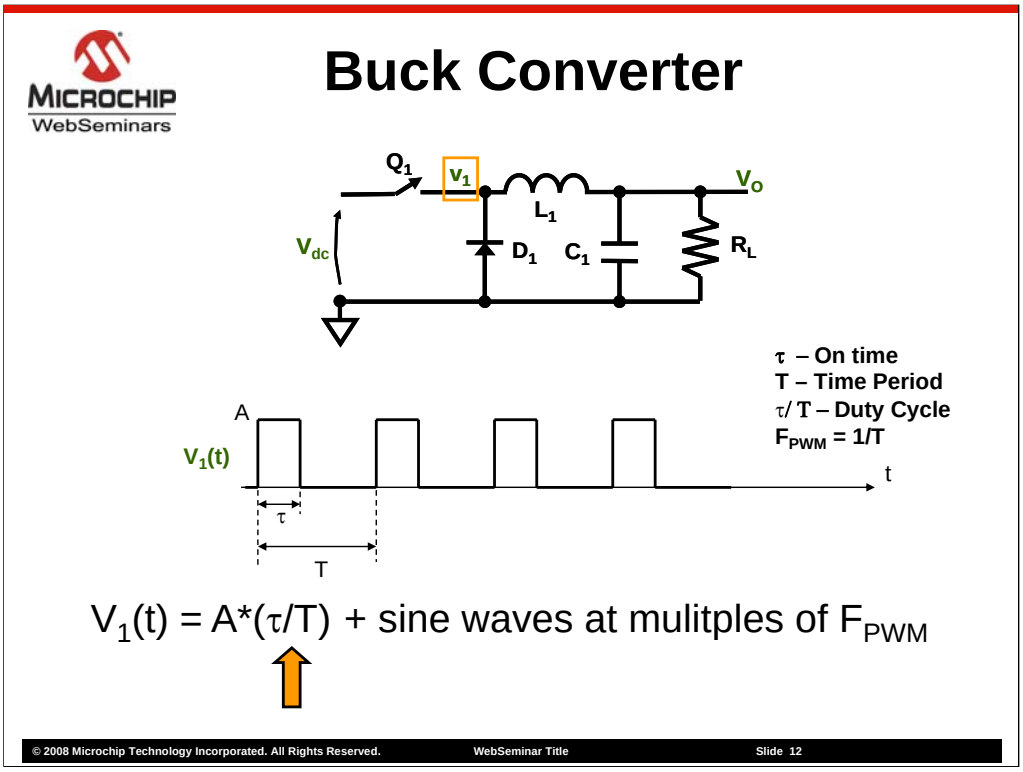
Here V_1 is shown as a time varying periodic signal with a period T and amplitude A.



The duty cycle of this switching waveform is the ratio of the on time time period "tao" to the total time period.

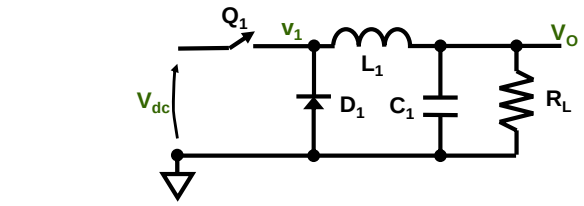


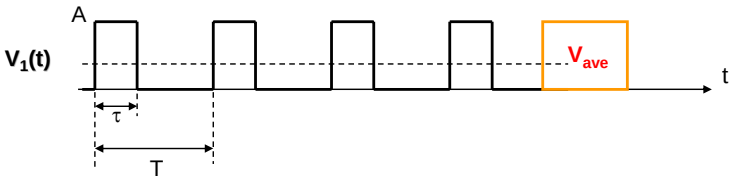
Using the Fourier Series Expansion for periodic signals, signal $V_1(t)$ can be expressed as the sum of a DC term and weighted sinusoidal signals at mulitples of the fundamental frequency.



As seen here, the DC term is proportional and dependant on the duty cycle of the switching waveform. This is the term that will be of interest to us in the next slide.

Buck Converter



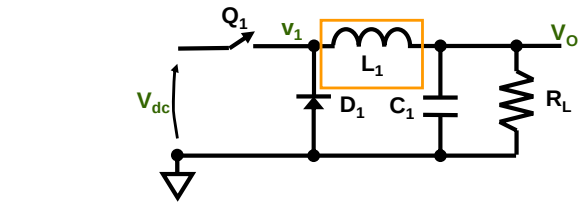


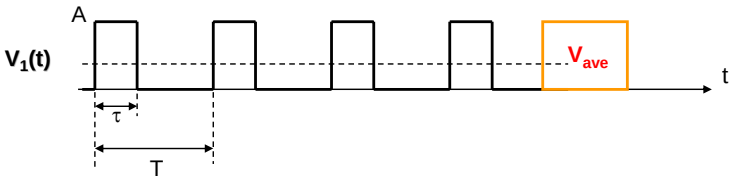
$V_1(t) = A*(\tau/T)$ + sinewaves at multiple frequency

 WebSeminar Title Slide 13

The DC term in the Fourier series expansion of $V_1(t)$ represents the average DC value of the switching waveform. The output of the buck converter should ideally be only this DC voltage. In order remove the high frequency components from $V_1(t)$, the signal needs to be filtered.

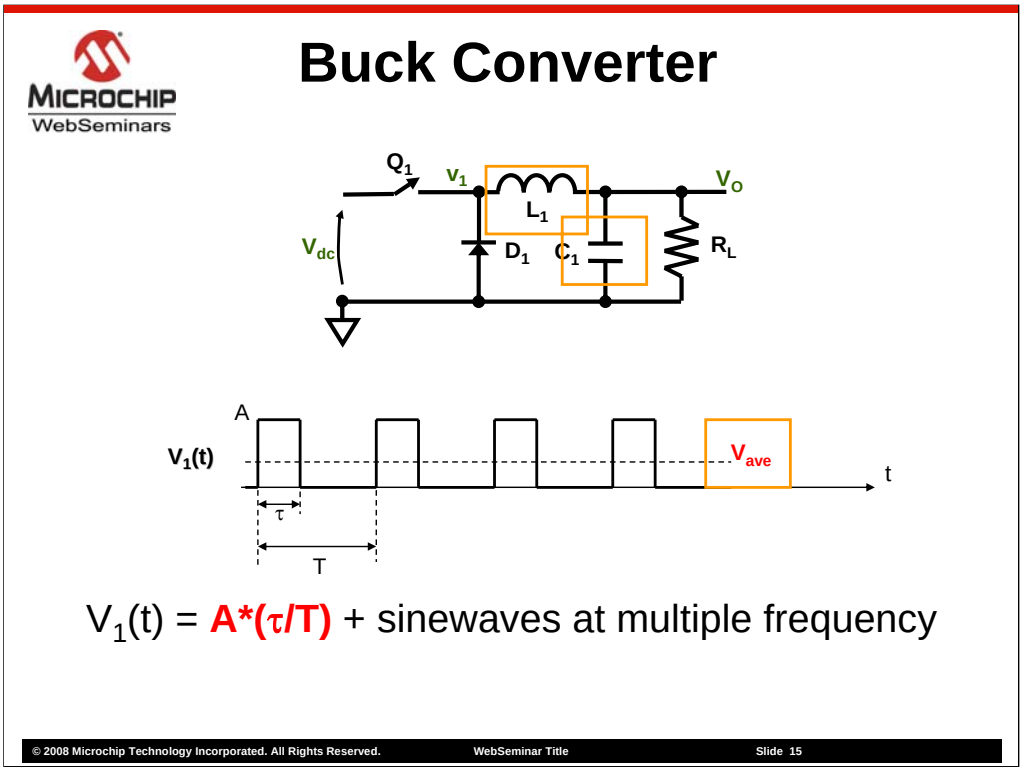
Buck Converter





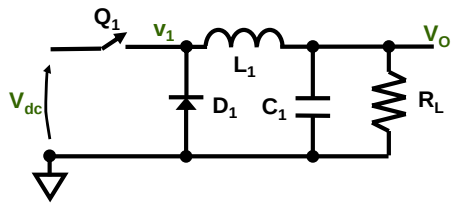
$V_1(t) = A*(\tau/T)$ + sinewaves at multiple frequency

This filtering function is performed by inductor L_1

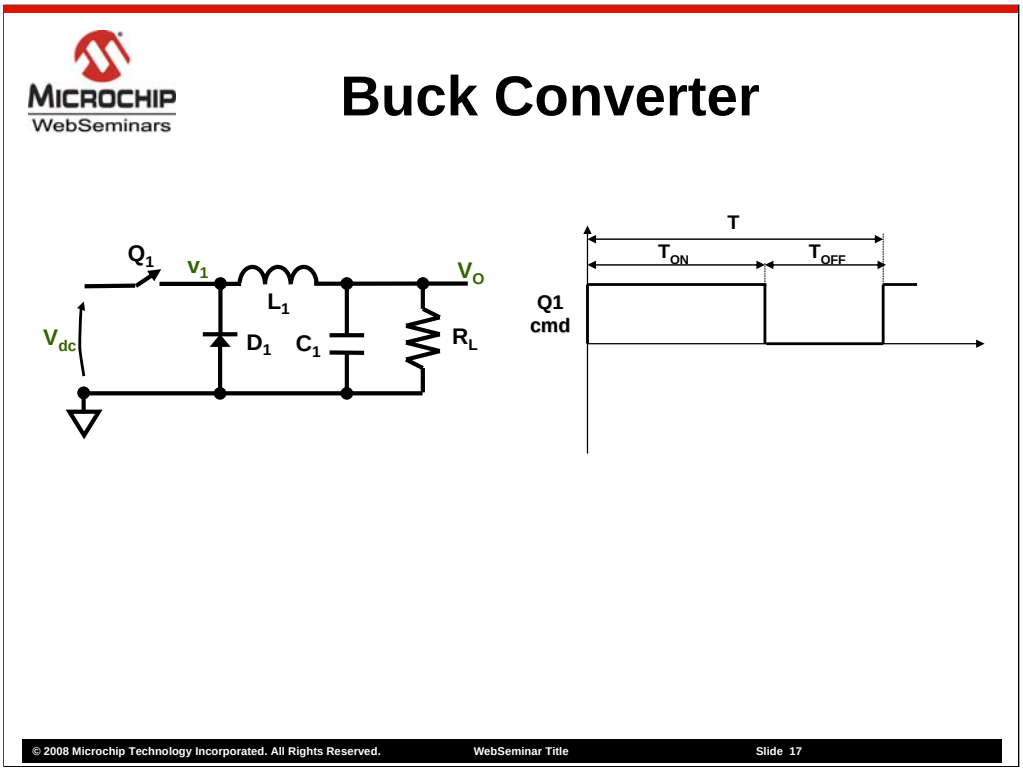


and capacitor C_1. The combined actioin of L_1 and C_1 will block the frequency dependant components and will only pass the DC component of the input signal. The general trend in the design of buck converters is to use high switching frequencies. This simplifies the filter design. The output of the low pass filter is the average voltage V_{ave}. Of course there are additional design constraints on the selection of L_1 and C_1: These are discussed in the subsequent slides.

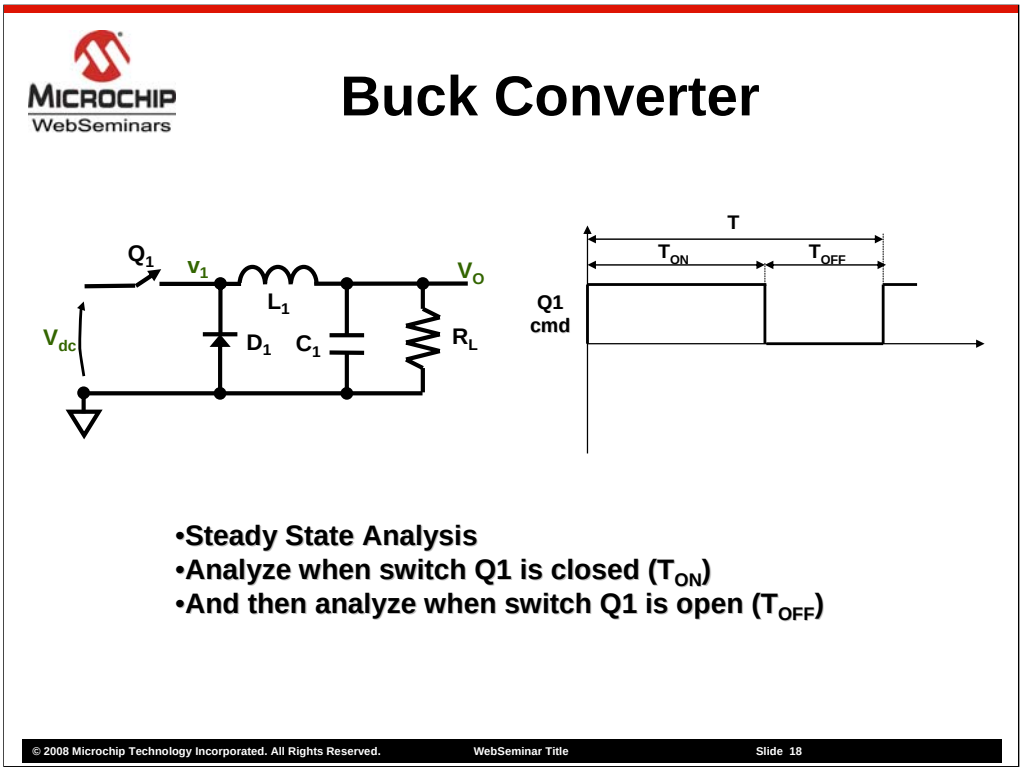
Buck Converter



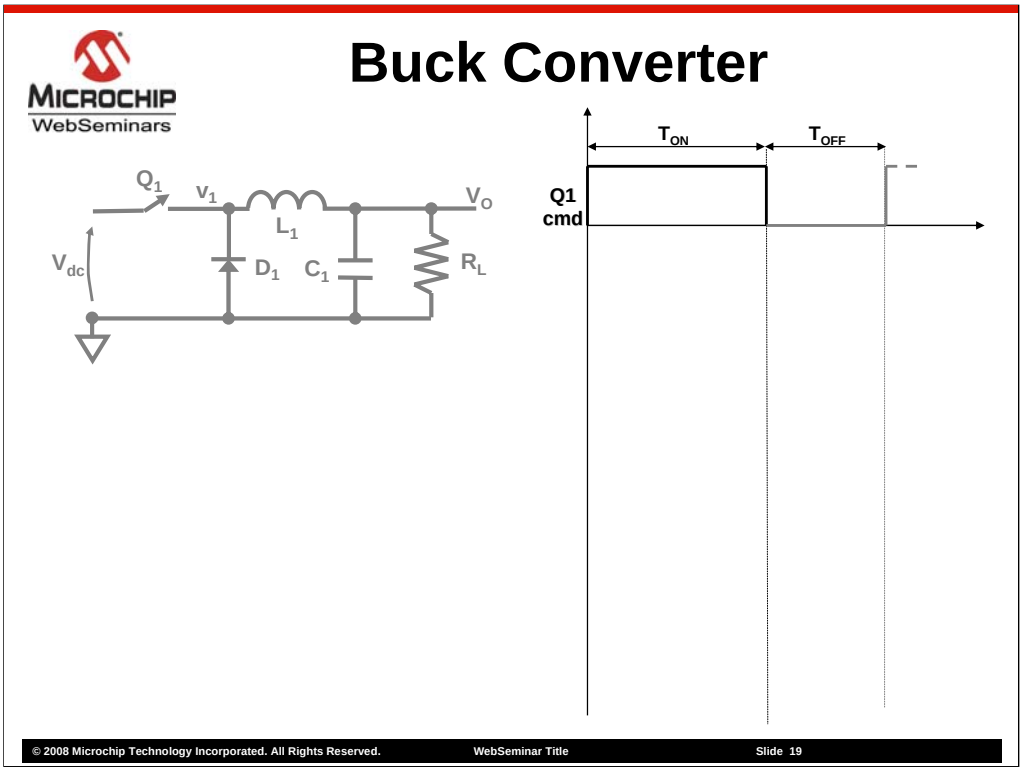
Let us examine the behavior of the buck convertor circuit when the switch Q_1 is closed, and when it is open.



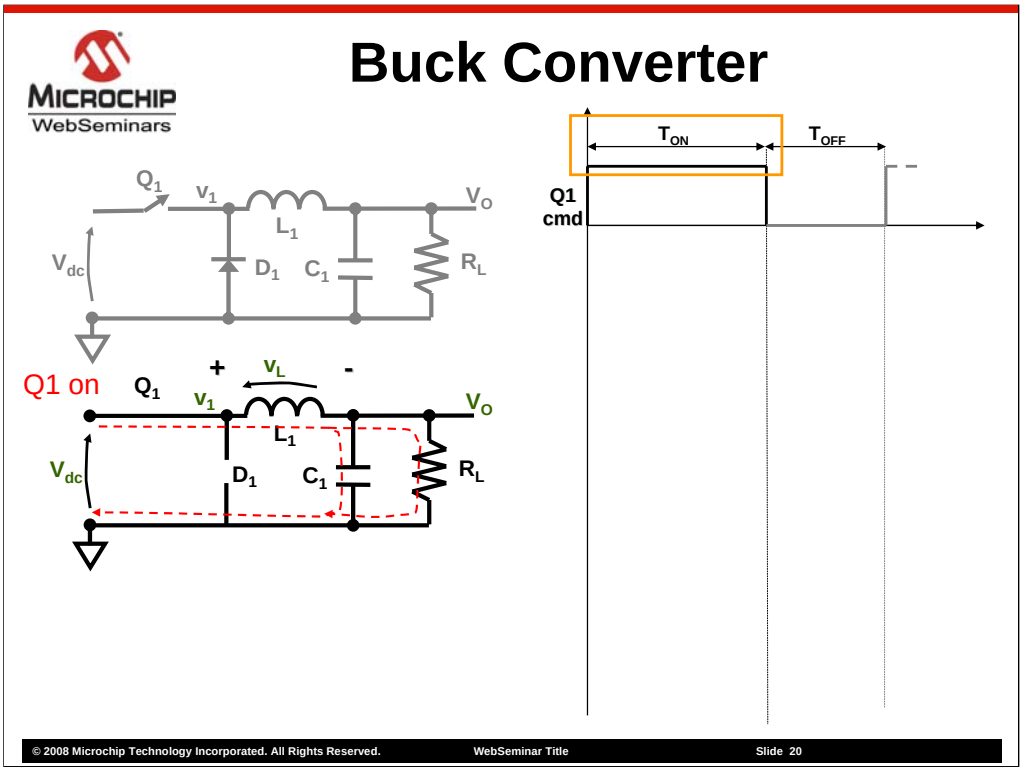
For our analysis we will assume that Q_1 is being controlled by a square wave signal as shown here. The square wave has variable duty cycle. The sum of T_{ON} and T_{OFF} makes the full switching period T. These control signals are usually generated by a PWM controller such as the PWM peripheral on the SMPS dsPIC DSC devices.



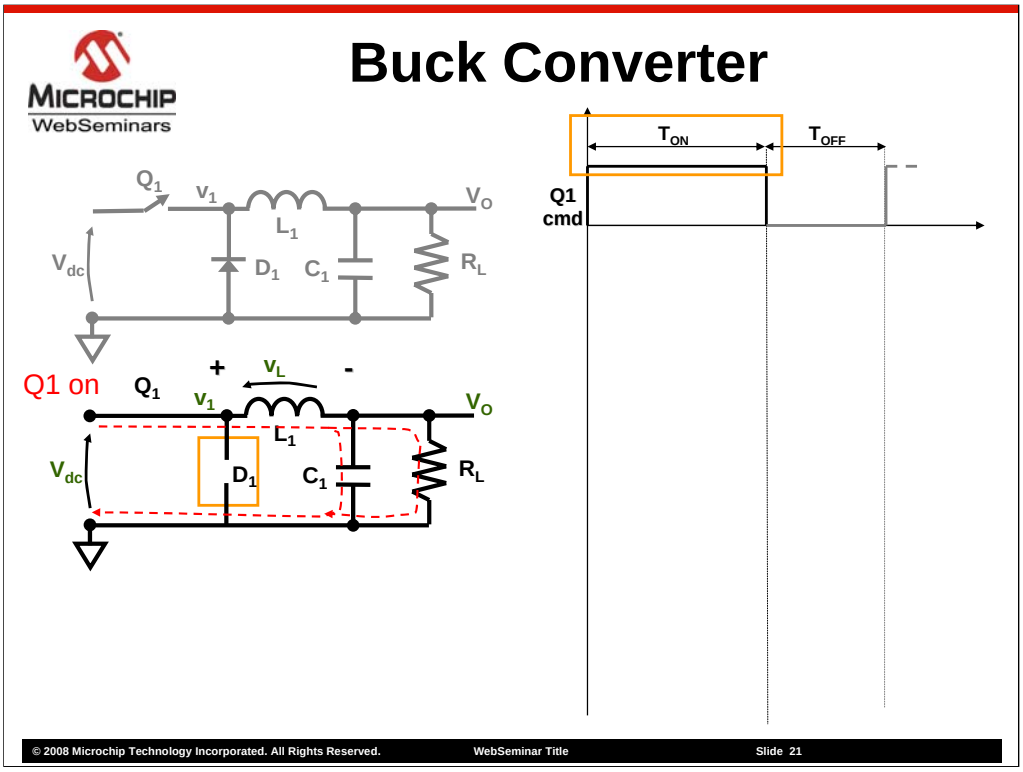
While analyzing the circuit, we will follow an approach which is typical to the study of such circuits. We assume that at the time of analysis, the circuit is already at steady state: all transients in the system have died down and the output voltage has already reached its final, nominal value, V_o. This approach is useful to understanding the general behavior of the circuit. The steady state analysis provides sufficient insight into the operation of the circuit. If needed, a more precise transient analysis can be carried out with software simulation tools



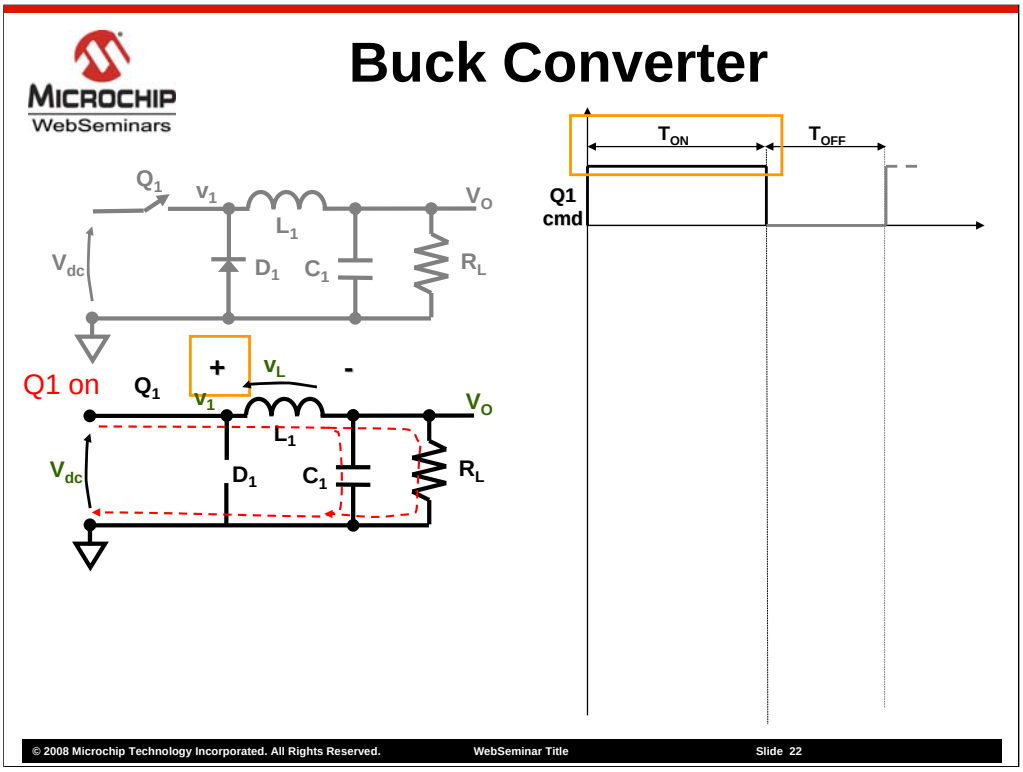
Let's analyse the buck convertor circuit when switch Q_1 is closed.



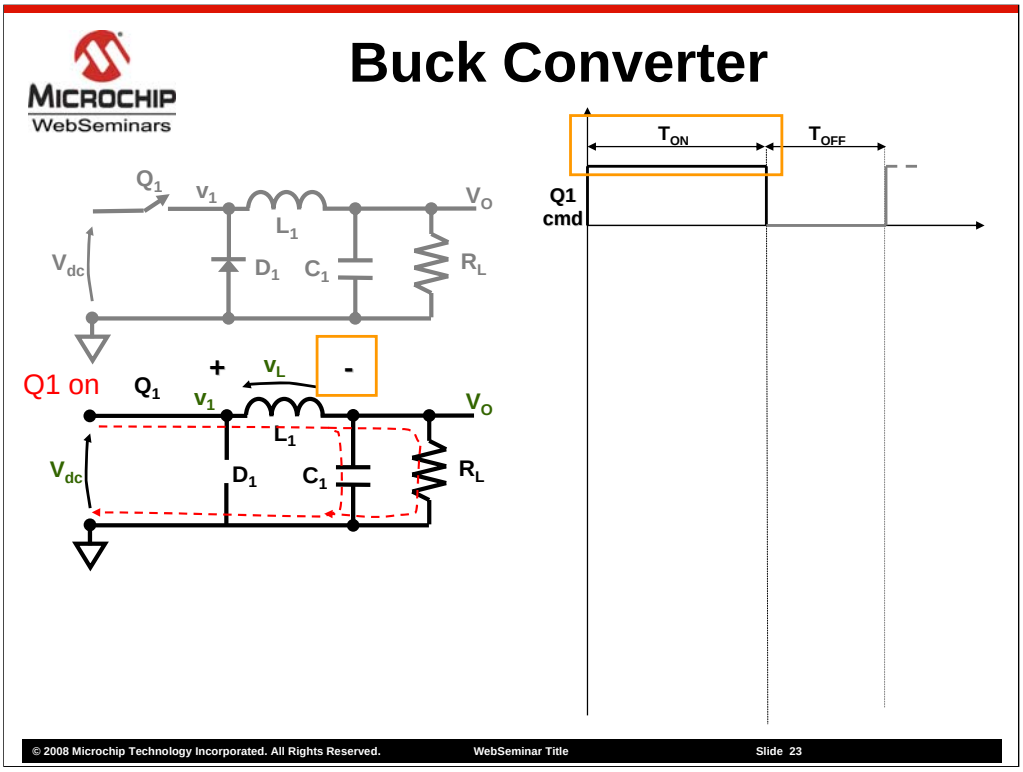
This happens during the time T_{ON}. The equivalent circuit is shown here. During this time, switch Q_1 is represented as a short circuit. In reality, the switch will have a small finite resistance which produces a voltage drop $V_{Q,ON}$.



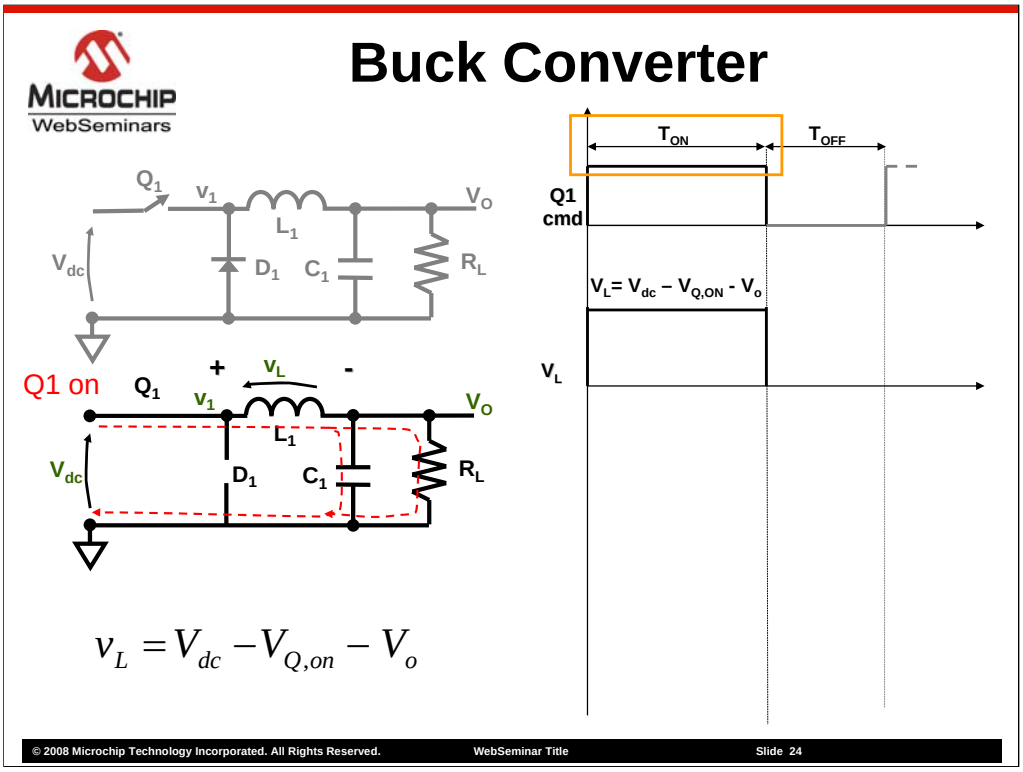
Diode D_1 is reverse-biased and is not conducting.



The left side of the inductor is more positive

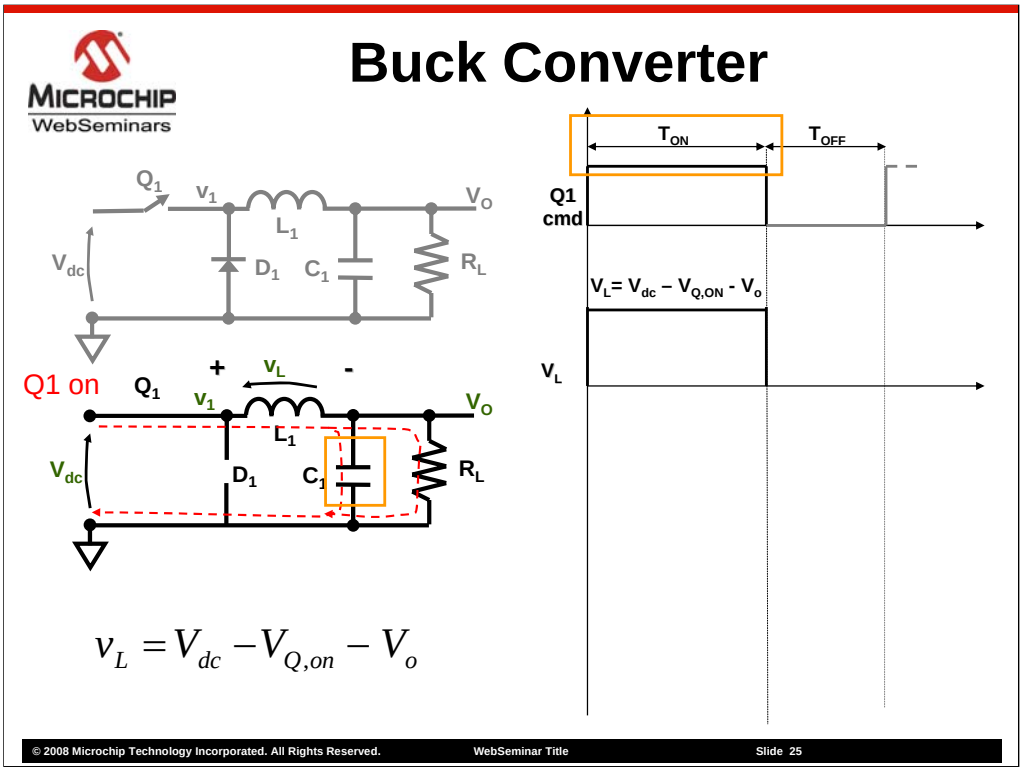


than the right side.

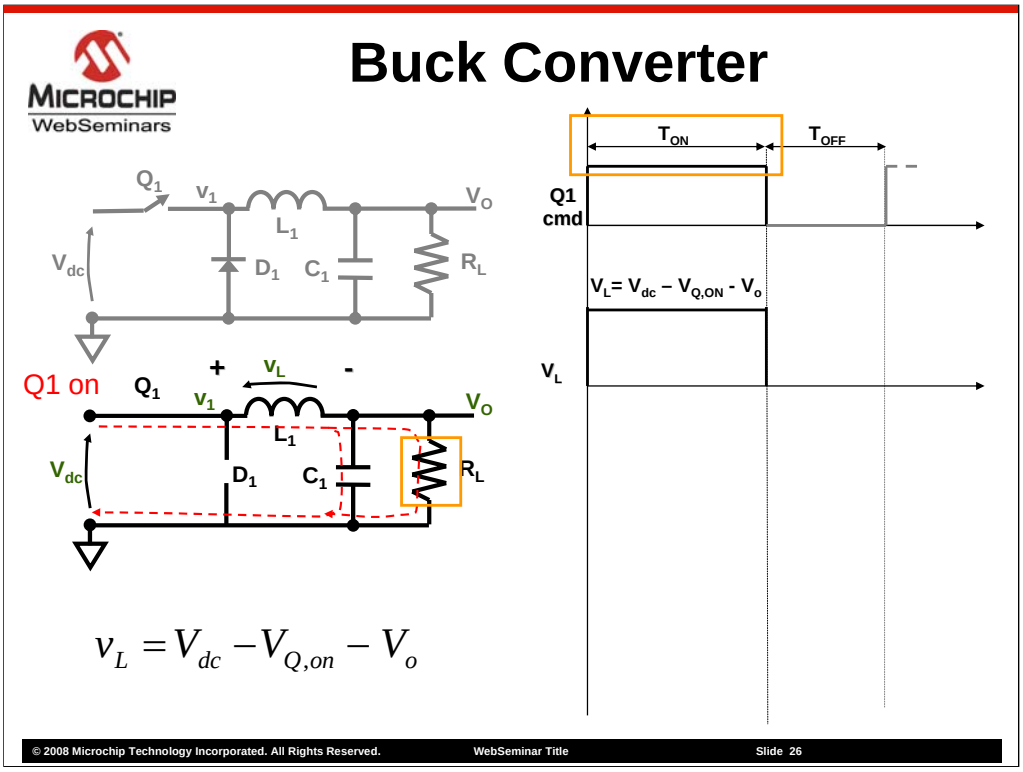


The voltage across the inductor is expressed as V_L. Since the circuit is already at steady state, voltage V_L can be expressed by the equation shown here. The voltage drop across the switch can often be neglected, since this voltage drop is very small compared to input and output voltage.

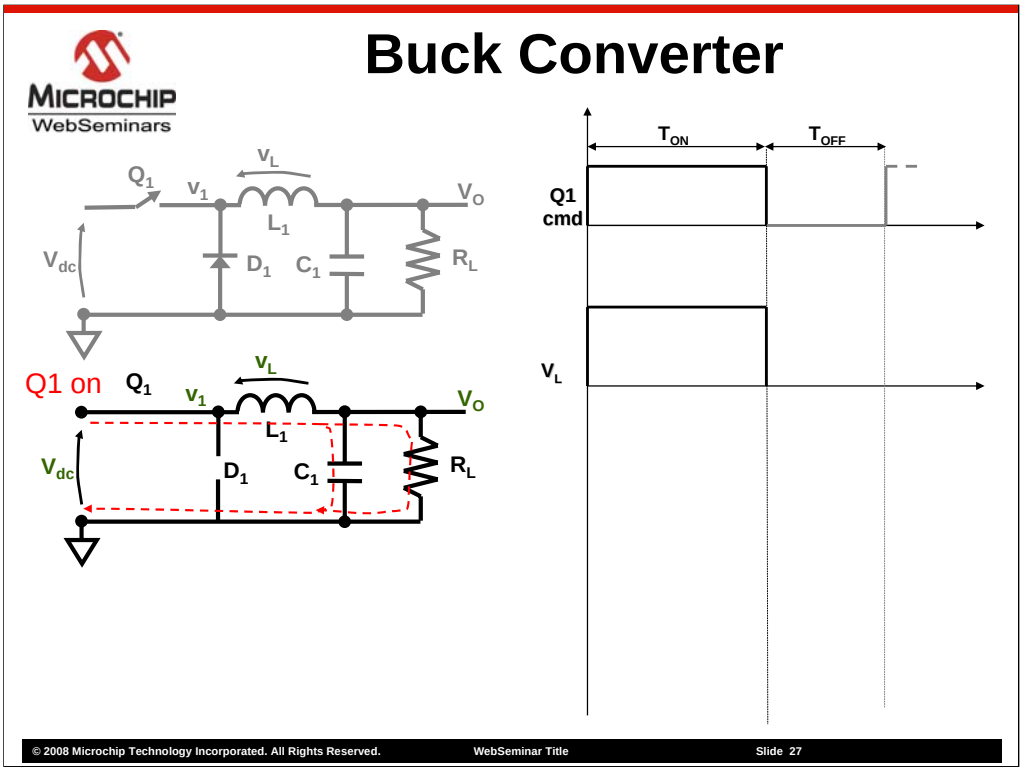
Some energy is stored in the magnetic field of the inductor. The current flow in the circuit is indicated by the red dotted lines.



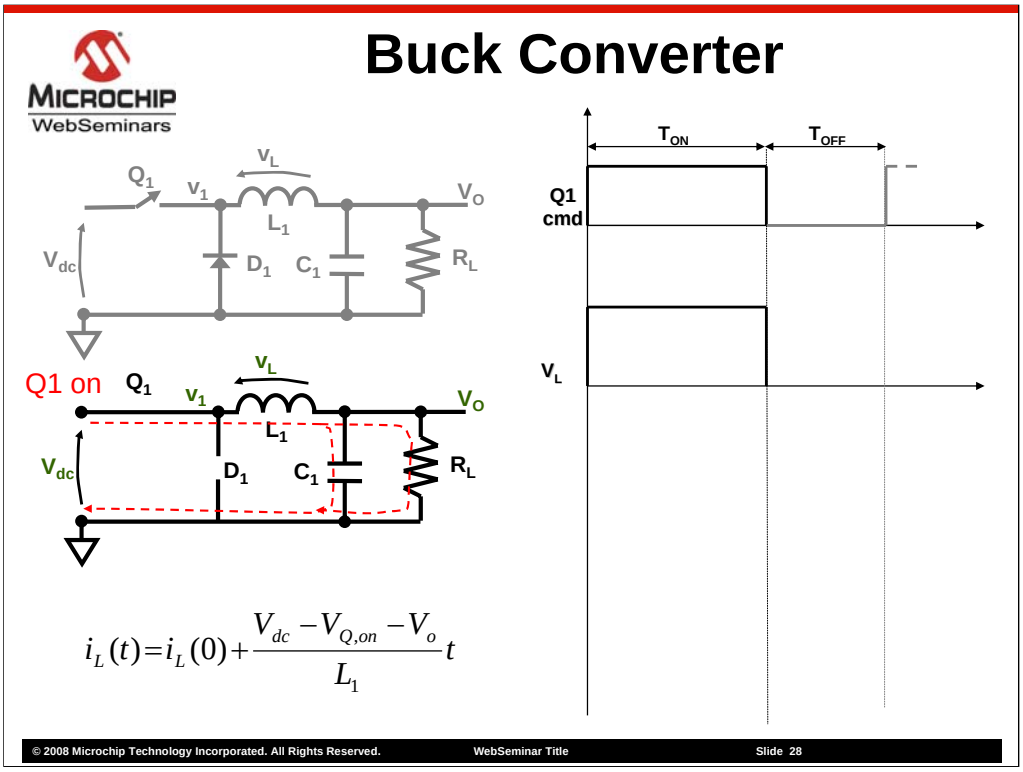
The current flows in two branches, one branch current charges the capacitor



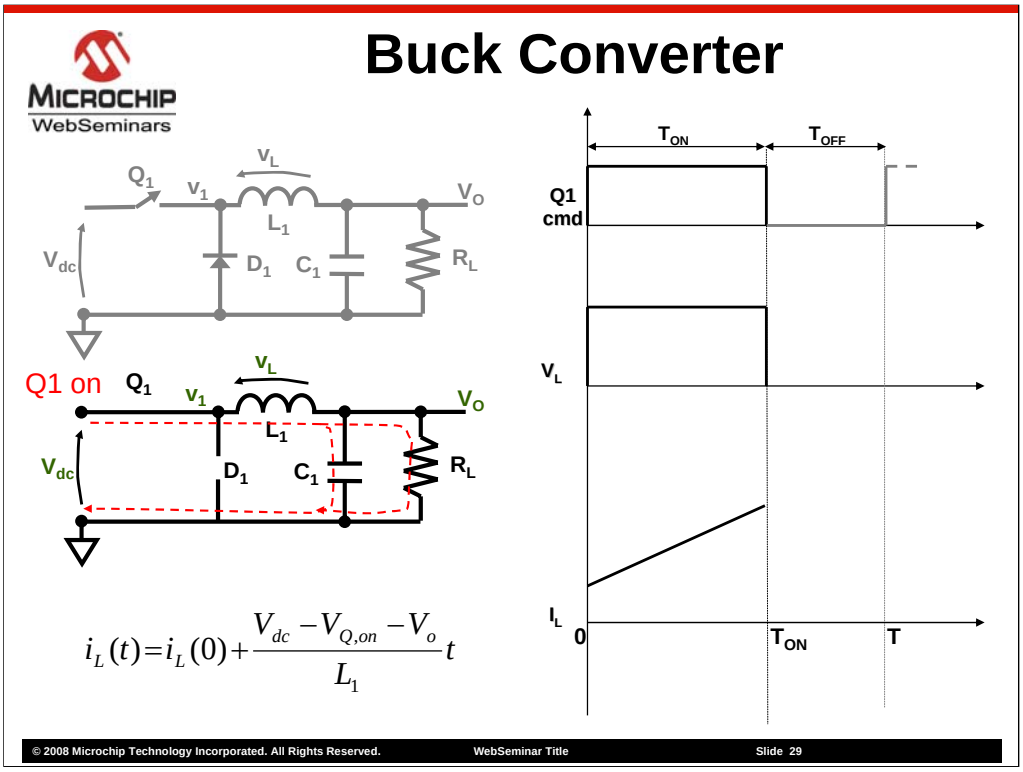
while the other branch current flows through the load.



The current flowing into the inductor is related to the inductor voltage

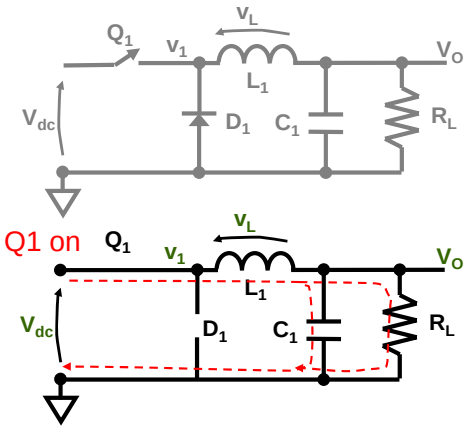


by the equation shown here. This reflects the property of the inductor, whereby it controls the rate at which the current flowing through it changes.



The inductor current displays a linear behavior with a rising slope during time T_{ON}. We will see later as to why the inductor current generally does not start from zero at the beginning of the period.

Buck Converter



Topology Equations

Inductor Voltage:

$$v_L = V_{dc} - V_{Q,on} - V_o \quad \text{...Eq. 1}$$

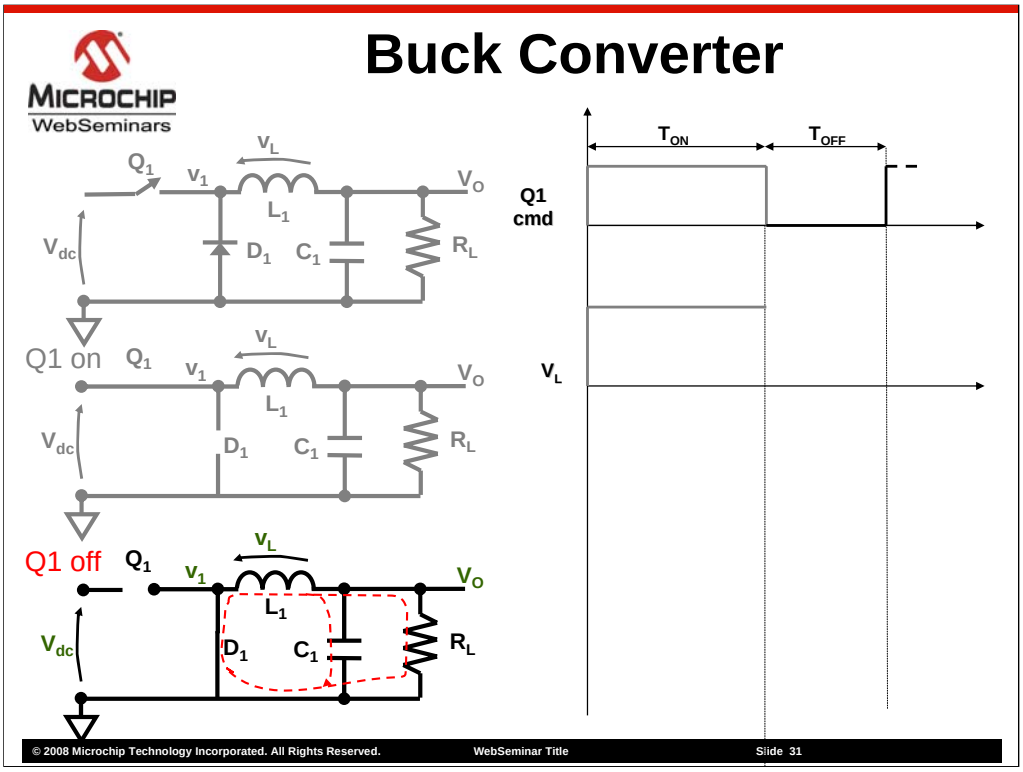
Inductor Current:

$$i_L(t) = i_L(0) + \frac{\left(V_{dc} - V_{Q,on} - V_o\right)}{L_1} t \quad \text{...Eq. 2}$$

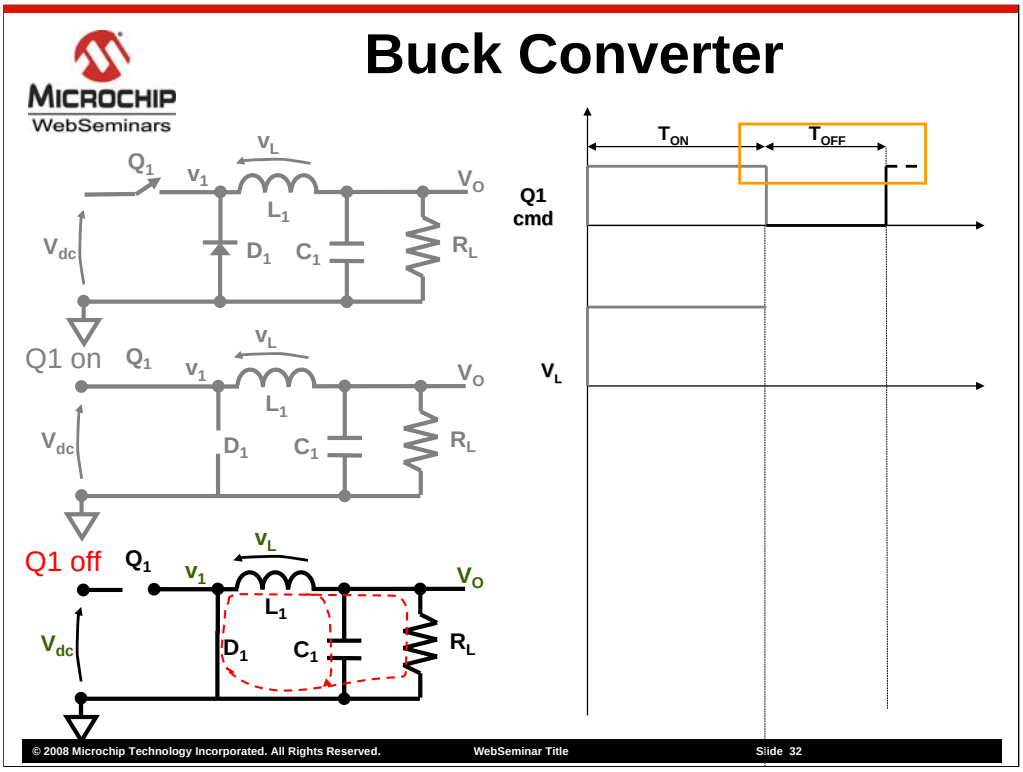
Inductor Current at T_{ON}:

$$i_L(T_{on}) = i_L(0) + \frac{\left(V_{dc} - V_{Q,on} - V_o\right)}{L_1} T_{on} \quad \text{...Eq. 3}$$

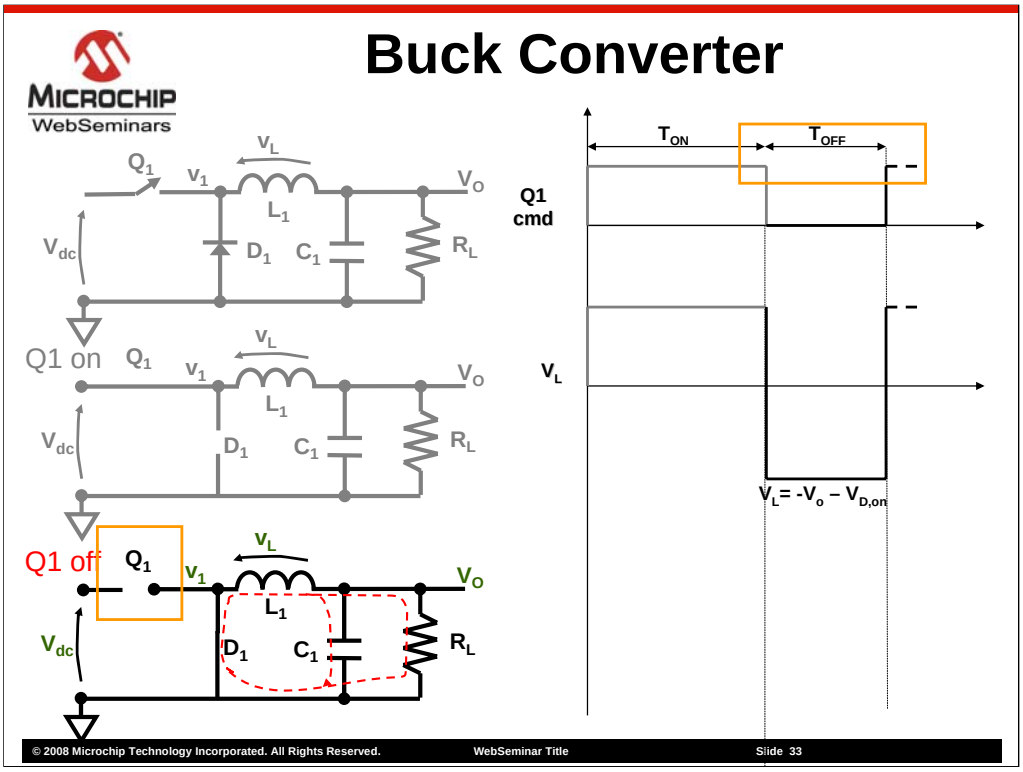
The three equations listed here summarize the operation of the circuit when switch Q_1 is on. Equation 1 gives the voltage across the inductor. Equations 2 and 3 specify the current through the inductor.



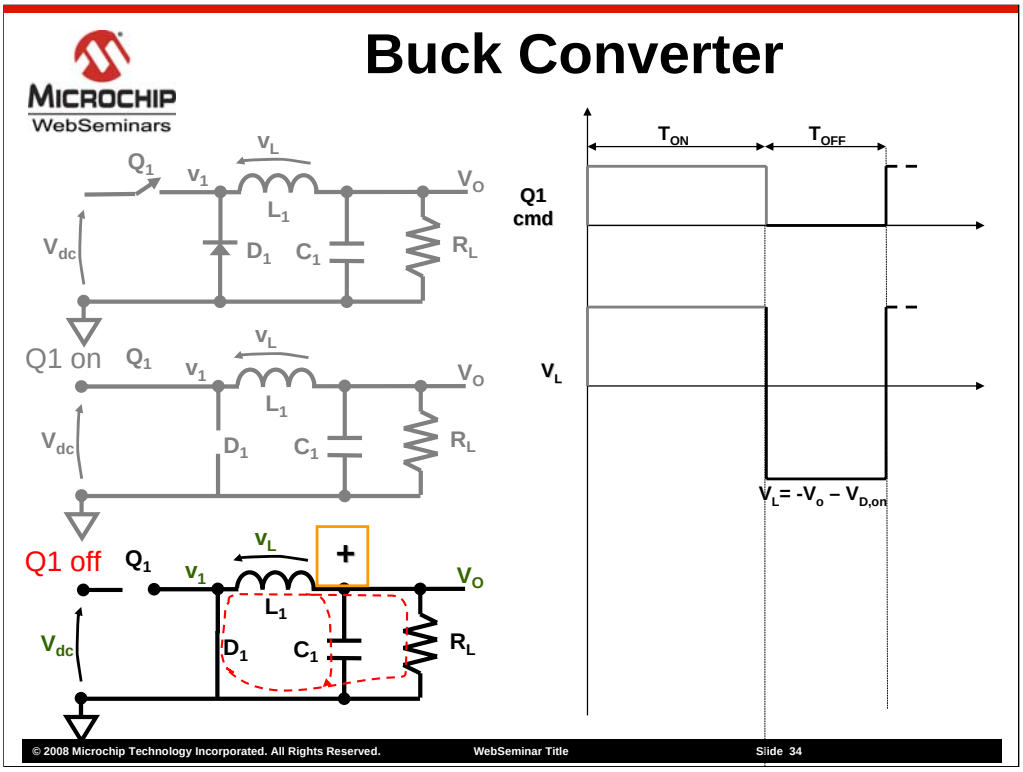
Lets analyze the circuit when switch Q_1 is off.



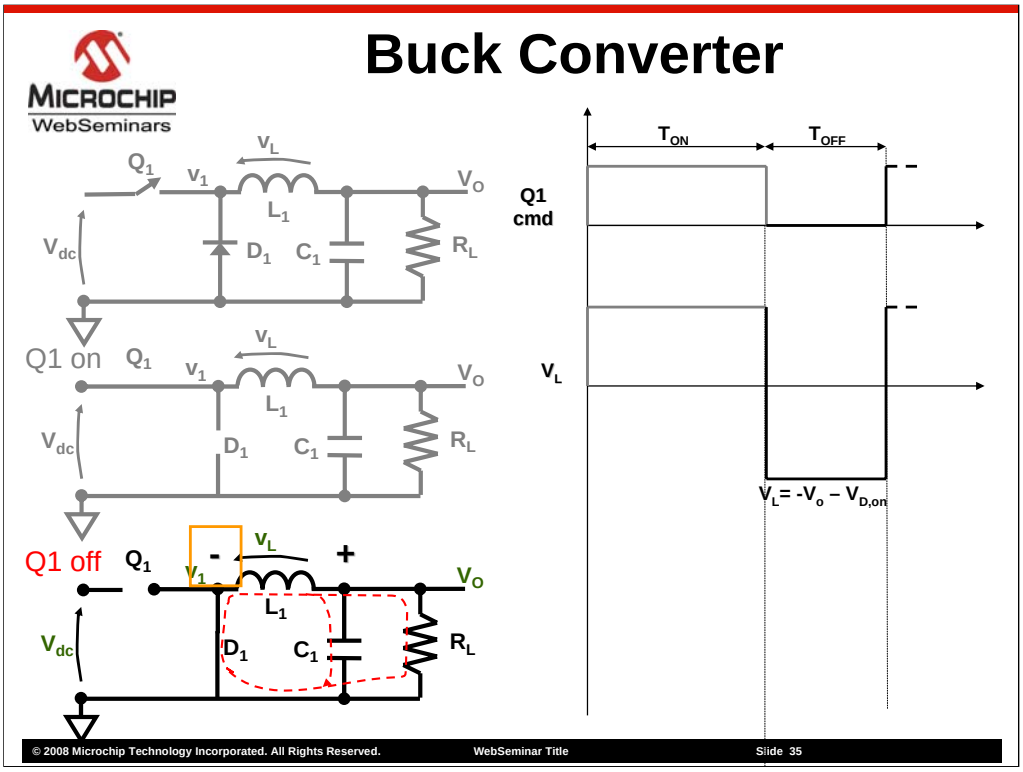
This happens during time T_{OFF}.



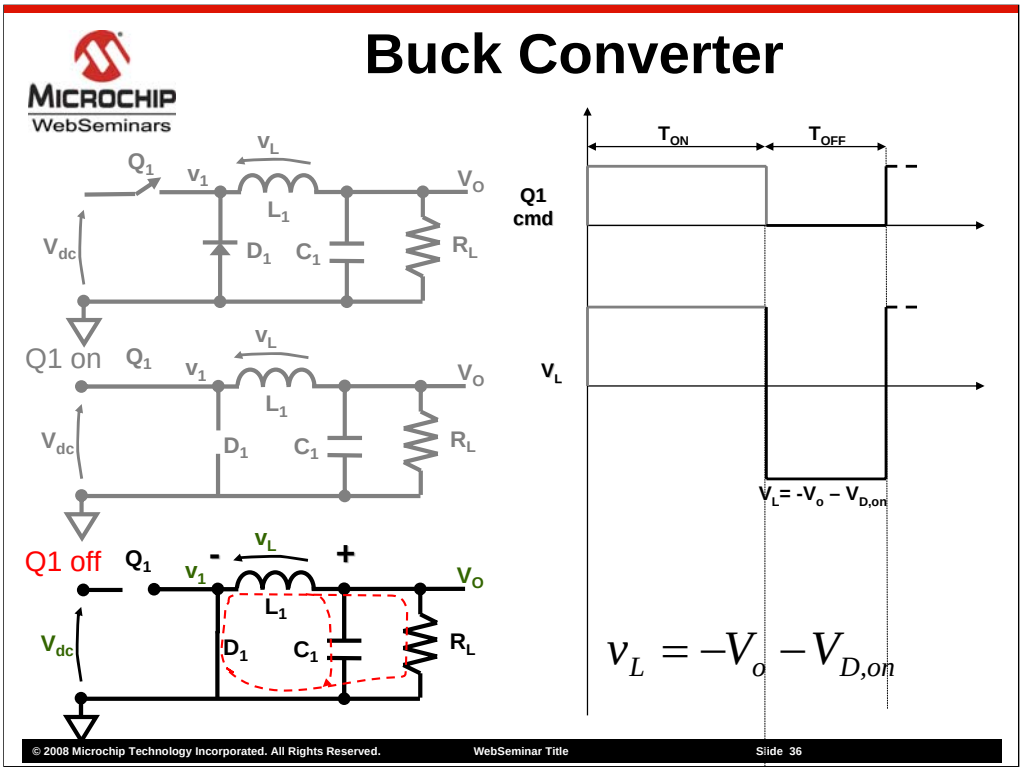
Switch Q_1 is replaced by an open circuit and the circuit is now disconnected from V_{dc}. By its basic property, the inductor will try to keep the current flowing in the same direction; however, this means that the voltage across the inductor will reverse polarity.



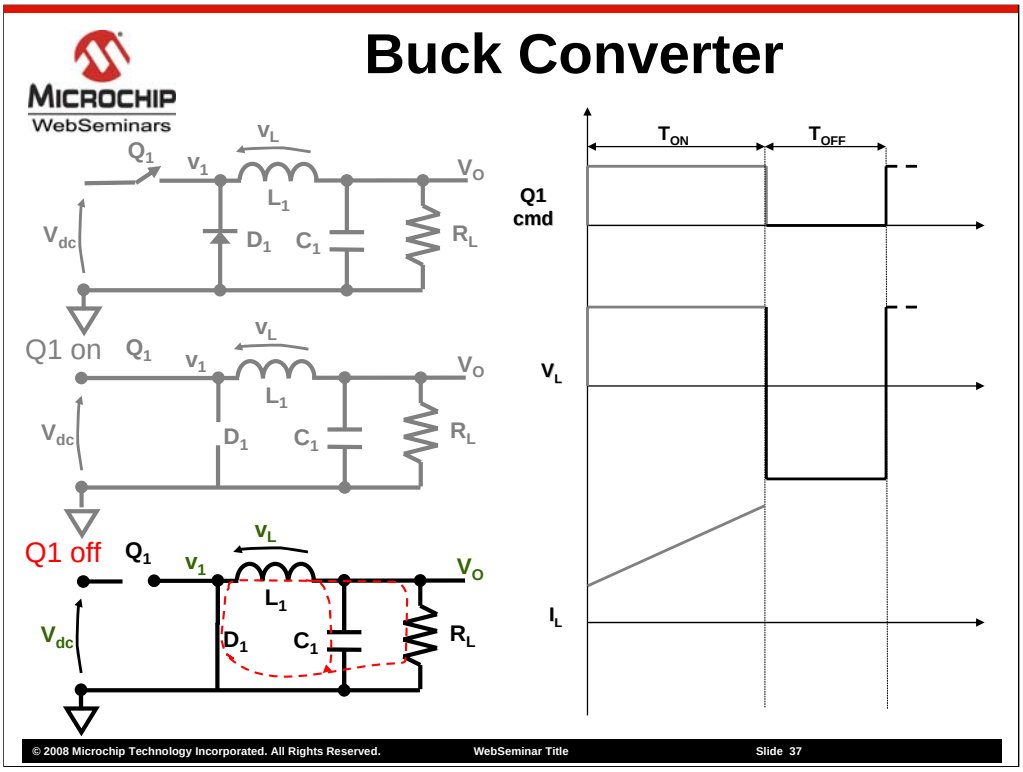
Now, the right side



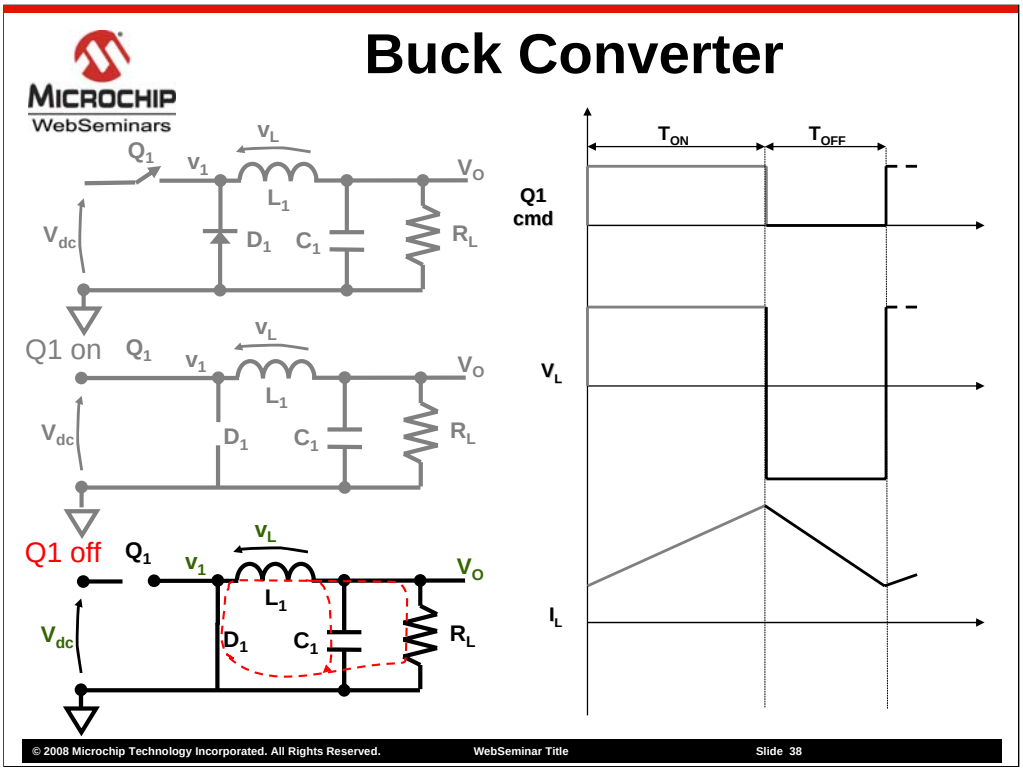
is more positive than the left side.



The voltage across the inductor V_L as shown here is now a sum of the output voltage V_o and the foward bias voltage across the diode. The voltage at Node V_1 will try to become more negative, but the freewheeling diode D_1 will prevent it from going lower than $V_{D,on}$. Note that the direction of current in the two branches has not changed. The inductor will still charge the capacitor and supply current to the load. The capacitor will also try to maintain a constant voltage across the load.

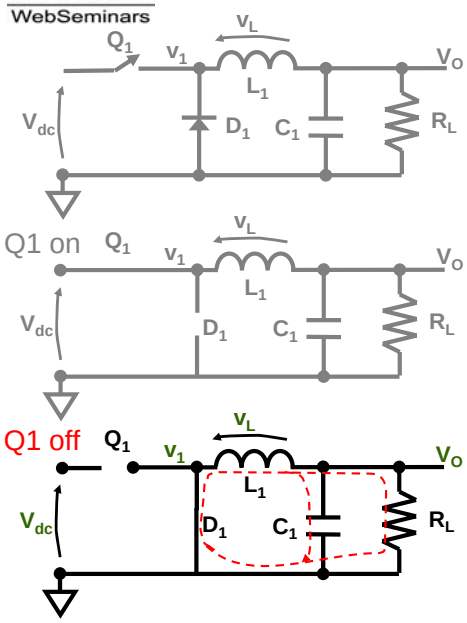


During time T_{OFF}, the current through the inductor, I_L,



will reduce linearly as seen here. This linear rise and fall of the current will repeat with every on and off cycle of switch Q_1.

Buck Converter



Topology Equations

Inductor Voltage:

$$v_L = -V_o - V_{D,on} \quad \text{...Eq. 4}$$

Inductor Currrent:

$$i_L(t) = i_L(T_{on}) + \frac{-V_o - V_{D,on}}{L_1} T_{off} \quad \text{...Eq. 5}$$

The equations summarizing the operation of the buck convertor circuit during the T_{OFF} period have shown here. Equation 4 expresses the voltage across the inductor and equation 5 express the current through the inductor.

Buck Converter – Current Ripple

At steady state:

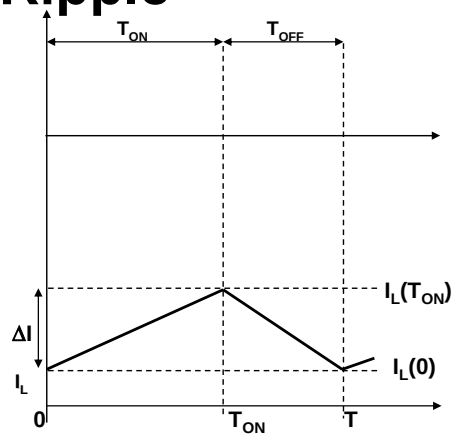
$i_L(0) = i_L(T)$

Then (current ripple):

$\Delta I = i_L(T_{ON}) - i_L(0)$

and (average current):

$I_{ave} = i_L(0) + (\Delta I / 2)$



Let's analyze the current flowing through the inductor during each PWM period. We will again take advantage of performing steady state analysis of the circuit.

Buck Converter – Current Ripple

At steady state:

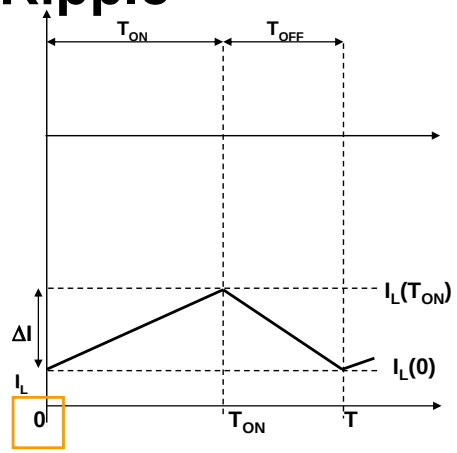
$i_L(0) = i_L(T)$

Then (current ripple):

$\Delta I = i_L(T_{ON}) - i_L(0)$

and (average current):

$I_{ave} = i_L(0) + (\Delta I / 2)$



In this condition, the current flowing into the inductor at the beginning of each pwm period

Buck Converter – Current Ripple

At steady state:

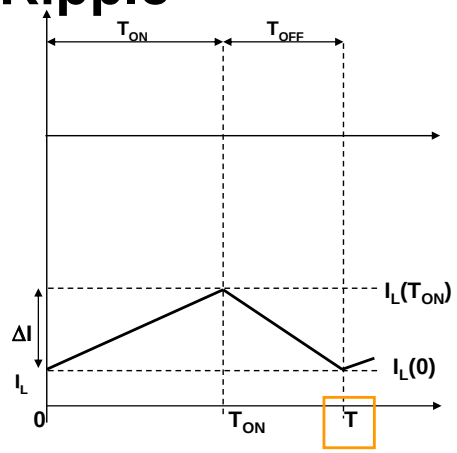
$i_L(0) = i_L(T)$

Then (current ripple):

$\Delta I = i_L(T_{ON}) - i_L(0)$

and (average current):

$I_{ave} = i_L(0) + (\Delta I / 2)$



must equal the current at the following end of the period. If this is not true, it means that the system has not yet reached a steady state condition , or some kind of perturbation has occurred.

Buck Converter – Current Ripple

At steady state:

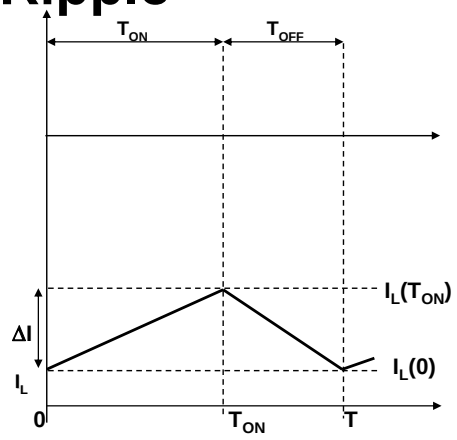
$i_L(0) = i_L(T)$

Then (current ripple):

$\Delta I = i_L(T_{ON}) - i_L(0)$

and (average current):

$I_{ave} = i_L(0) + (\Delta I / 2)$



In the steady state, the current ripple is therefore expressed as the maximum change in the current amplitude during the cycle. If we assume the capacitor across the load to be ideal, then it will filter out this ripple. We will discuss this in more detail later.

Buck Converter – Current Ripple

At steady state:

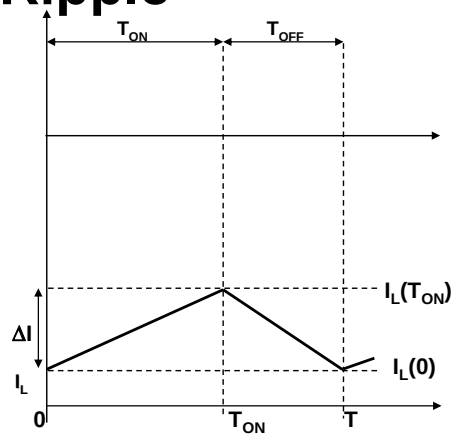
$i_L(0) = i_L(T)$

Then (current ripple):

$\Delta I = i_L(T_{ON}) - i_L(0)$

and (average current):

$I_{ave} = i_L(0) + (\Delta I / 2)$

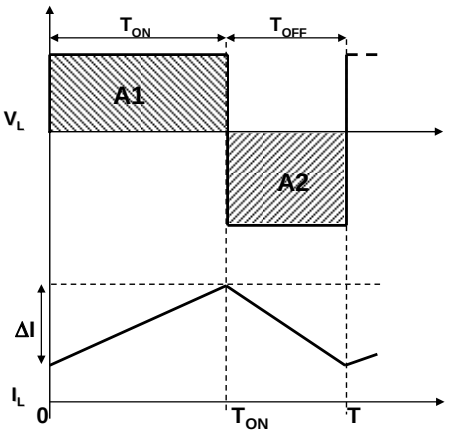


The average value of the inductor current is then expressed as the sum of the current at the beginning of the period and one/half of the ripple value. By the virtue of this topology, the average current flowing through the inductor is also the average current flowing though the load.

Buck Converter – Input/Output Relationship

From $A_1 = A_2$:

$$(V_{dc} - V_{Q,on} - V_o)T_{on} = (V_o + V_{D,on})T_{off}$$



consequently:

$$V_o = D\,V_{dc} \quad where \quad D = \frac{T_{ON}}{T}$$

Since the voltage across the inductor is constant during T_{ON} and T_{OFF}, this results in a linear rise and fall of current through the inductor. When the system has reached steady state the rate at which the current rises during T_{ON} will equal the rate at which the current will decrease during T_{OFF}.

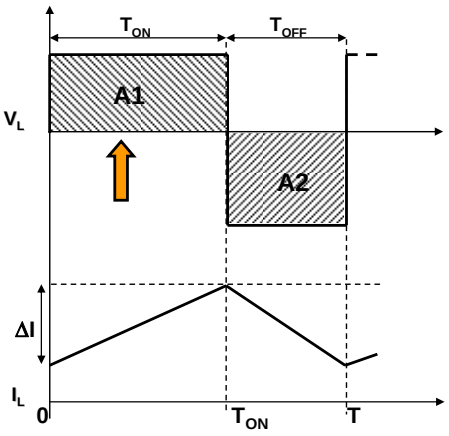
Buck Converter – Input/Output Relationship

From $A_1 = A_2$:

$$(V_{dc} - V_{Q,on} - V_o)T_{on} = (V_o + V_{D,on})T_{off}$$

consequently:

$$V_o = D\,V_{dc} \quad where \quad D = \frac{T_{ON}}{T}$$



This also implies that area A1

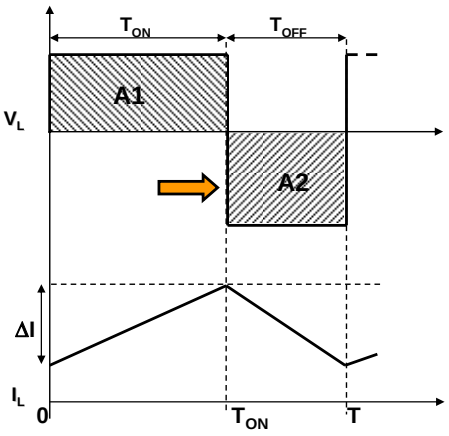
Buck Converter – Input/Output Relationship

From $A_1 = A_2$:

$$(V_{dc} - V_{Q,on} - V_o)T_{on} = (V_o + V_{D,on})T_{off}$$

consequently:

$$V_o = D\,V_{dc} \quad where \quad D = \frac{T_{ON}}{T}$$



must equal area A2.

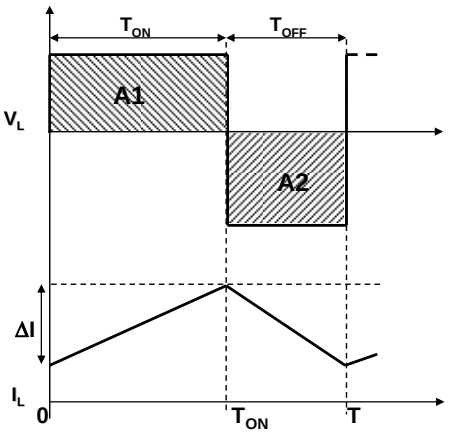
Buck Converter – Input/Output Relationship

From $A_1 = A_2$:

$$(V_{dc} - V_{Q,on} - V_o)T_{on} = (V_o + V_{D,on})T_{off}$$

consequently:

$$V_o = D\,V_{dc} \quad where \quad D = \frac{T_{ON}}{T}$$

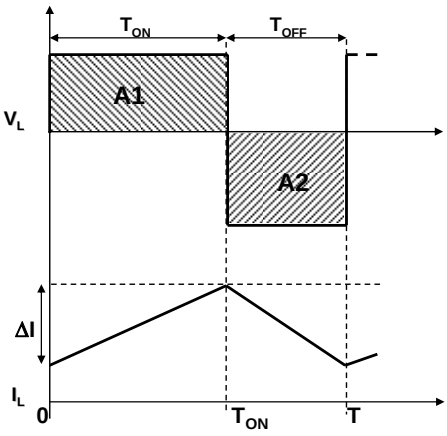


By re-arranging the equations shown here, and neglecting for simplicity the voltage drops across the diode and the switch, we get a linear relationship between input and output.

Buck Converter – Input/Output Relationship

From $A_1 = A_2$:

$$(V_{dc} - V_{Q,on} - V_o)T_{on} = (V_o + V_{D,on})T_{off}$$



consequently:

$$V_o = D\,V_{dc} \quad where \quad D = \frac{T_{ON}}{T}$$

The proportionality constant is the duty cycle D, which is the ratio T_{ON}/T.

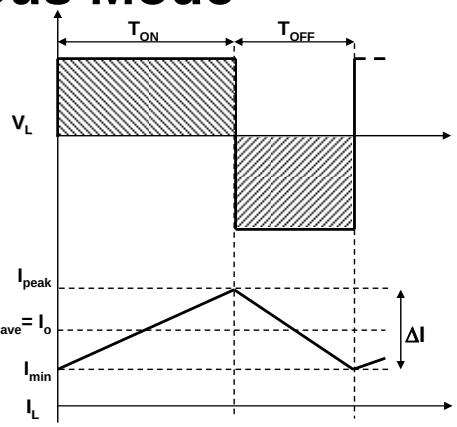
Buck Converter – Continuous Mode

Defined by the condition:

$I_{min} > 0$

Note that:

$I_{ave} = I_{min} + (\Delta I / 2)$



So far, we have discussed the operation of the buck converter circuit in the so-called Continuous mode.

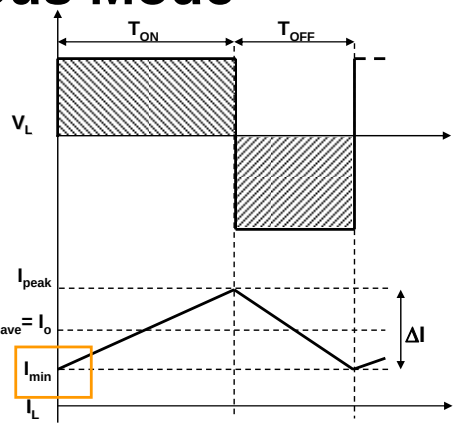
Buck Converter – Continuous Mode

Defined by the condition:

$I_{min} > 0$

Note that:

$I_{ave} = I_{min} + (\Delta I / 2)$



In this mode the inductor current is always greater than zero and there is always a continuous flow of current through the inductor. As seen in this figure, the value of I_{min} in the continuous mode is always greater than zero.

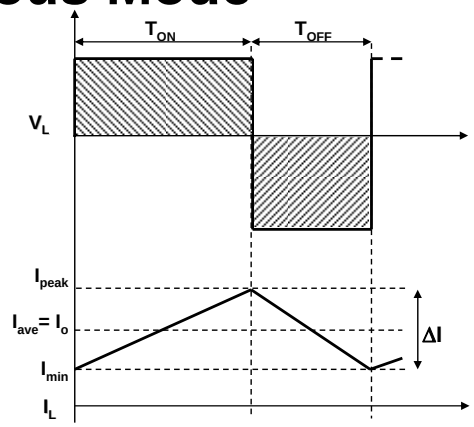
Buck Converter – Continuous Mode

Defined by the condition:

$I_{min} > 0$

Note that:

$I_{ave} = I_{min} + (\Delta I / 2)$

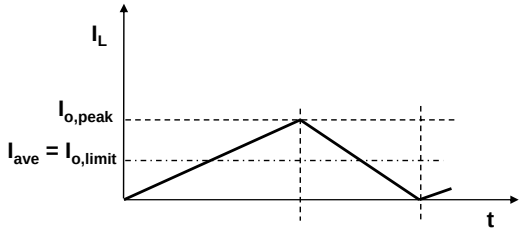


The average current flowing into the inductor is equal to the sum of the minimum current and one-half the peak current. One of the advantages of continuous mode, as seen in the past few slides, is that the relationship between the input and output voltage is linear.

The buck converter can also be operated in two other modes.

1. Critical mode
2. Discontinuous mode

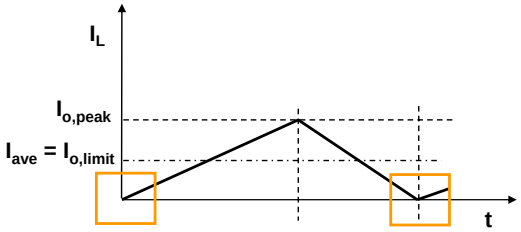
Buck Converter – Critical Mode



$$I_{o,limit} = I_{ave} = I_{o,peak} / 2$$

When the converter is operating in Critical mode,

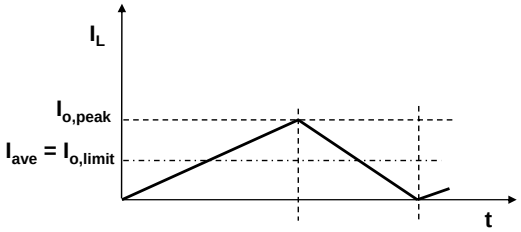
Buck Converter – Critical Mode



$$I_{o,limit} = I_{ave} = I_{o,peak} / 2$$

the inductor current reaches zero at the beginning and the end of each PWM period.

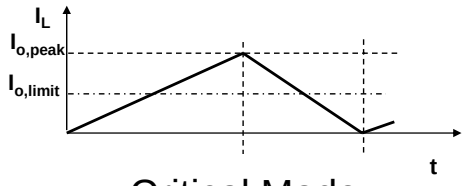
Buck Converter – Critical Mode



$$I_{o,limit} = I_{ave} = I_{o,peak} / 2$$

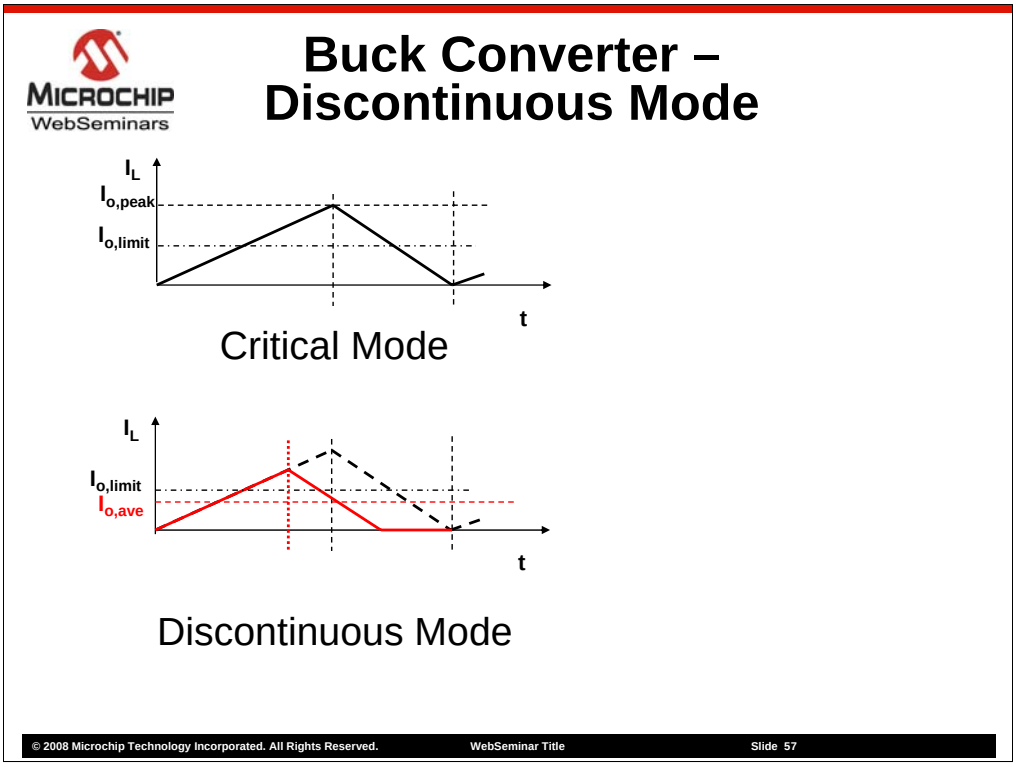
The average inductor current value when the system is in Critical mode is called limit current and equals one-half the peak current.

Buck Converter – Discontinuous Mode



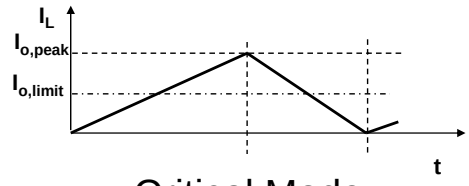
Critical Mode

As seen in the previous slide, in the critical mode the inductor current equals zero at the start and the end of the PWM period.

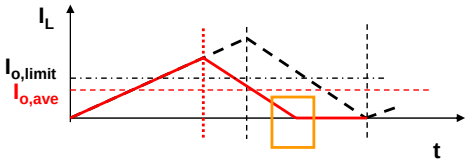


In the discontinuous mode,

Buck Converter – Discontinuous Mode

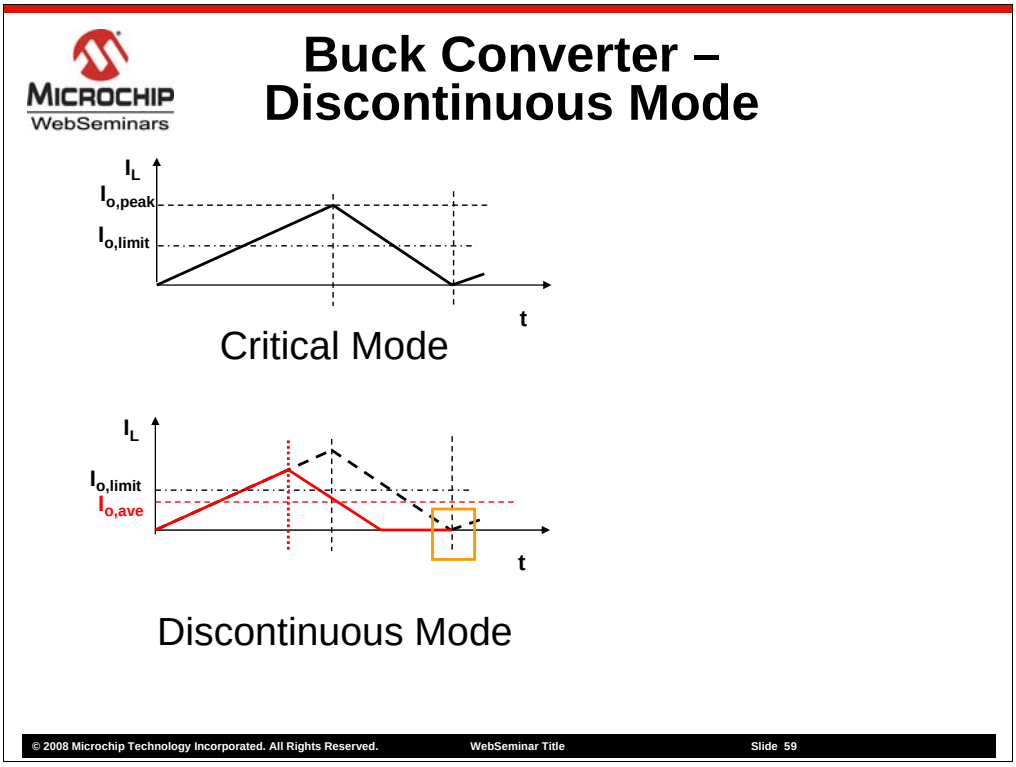


Critical Mode



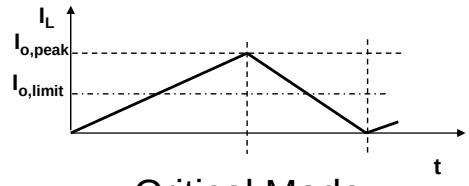
Discontinuous Mode

the inductor current reaches zero

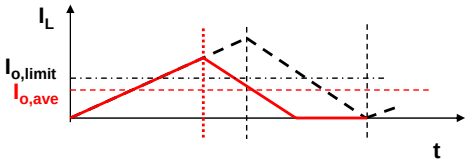


before the end of the PWM period. The discontinuous mode inductor current is shown here in red.

Buck Converter – Discontinuous Mode



Critical Mode



Discontinuous Mode

Input / Output Relationship

$$\frac{V_o}{V_{dc}} = \frac{D^2}{D^2 + \frac{1}{4}\left(I_o / I_{o,limit}\right)}$$

In this mode the output current $I_{o,ave}$ is lower than the current $I_{o,limit}$. The immediate consequence of this behavior is that the relationship between input and output voltage is no longer linear.

A buck converter can be designed to operate in Continuous, Discontinuous, or both modes. When designing converters which use both modes, care must be taken to ensure that the controller i.e. the system which keeps the output volatge constant is designed to cope with the different operating modes.

Buck Converter - Design

Known Quantities

- V_{dcmin} and V_{dcmax}
- Required output Voltage V_o
- Nominal load current $I_{o,av,nom}$
- PWM Frequency F_{PWM}
- Maximum Allowable Output Ripple.

We will now discuss the design of a buck converter, that is determining the components values. Before we start, we need to specify some data which will guide our design. We need to specify the minimum and maximum input voltage, output voltage , the required load current, the PWM frequency and finally the acceptable value of output ripple.

Buck Converter Design – Duty Cycle limit

Input-output relation:

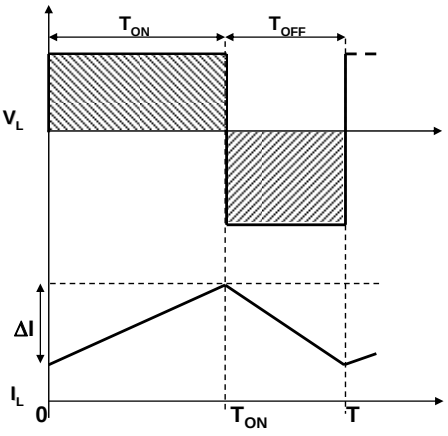
$$(V_{dc} - V_{Q,on} - V_o)T_{on} = (V_o + V_{D,on})T_{off}$$

consequently:

$$V_o = D\,V_{dc} \quad where \quad D = \frac{T_{ON}}{T}$$

Maximum duty cyle:

$$D_{\max} = \frac{V_o}{V_{dc,\min}}$$



From the input-output relationship it is easy to see that,

Buck Converter Design – Duty Cycle limit

Input-output relation:

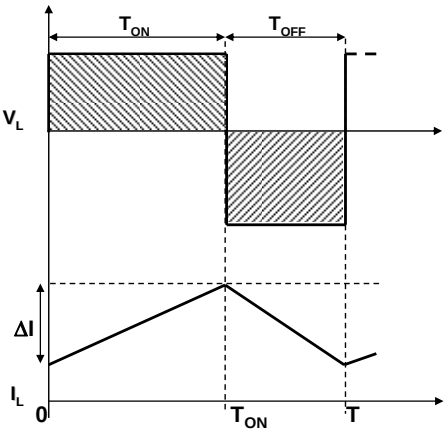
$$(V_{dc} - V_{Q,on} - V_o)T_{on} = (V_o + V_{D,on})T_{off}$$

consequently:

$$V_o = D\,V_{dc} \quad where \quad D = \frac{T_{ON}}{T}$$

Maximum duty cyle:

$$D_{\max} = \frac{V_o}{V_{dc,\min}}$$



once the output voltage has been defined, the maximum duty cycle in the system will be reached when the input voltage is at its minimum.

Buck Converter Design – Duty Cycle limit

Input-output relation:

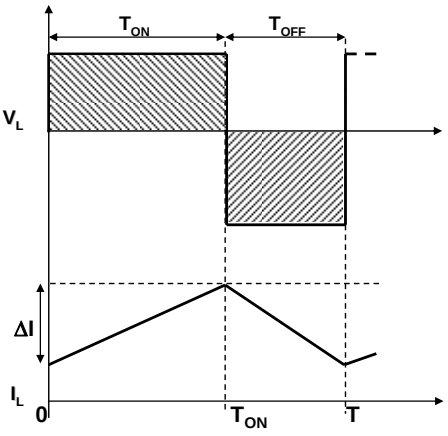
$$(V_{dc} - V_{Q,on} - V_o)T_{on} = (V_o + V_{D,on})T_{off}$$

consequently:

$$V_o = D\,V_{dc} \quad where \quad D = \frac{T_{ON}}{T}$$

Maximum duty cyle:

$$D_{\max} = \frac{V_o}{V_{dc,\min}}$$



The corresponding equation allows us to determine what the maximum duty cycle will be.

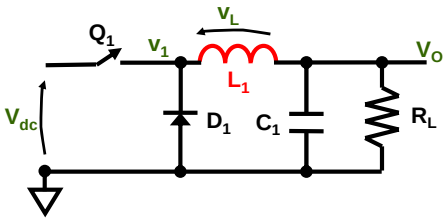
Buck Converter Design – Inductor

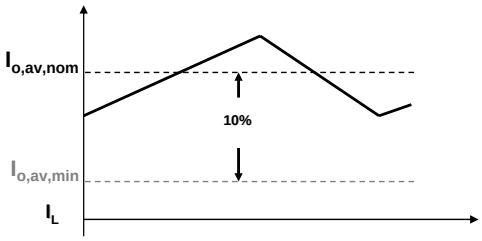
$$I_{o,av,\min} = 0.1 I_{o,av,nom}$$

$$I_{o,av,\min} = 0.1 I_{o,av,nom} = \frac{(V_{dc,nom} - V_o)}{2L_1} T_{on}$$

Solving

$$L_1 = \frac{5(V_{dc,nom} - V_o)V_o}{V_{dc,nom} F_{PWM} I_{o,av,nom}}$$

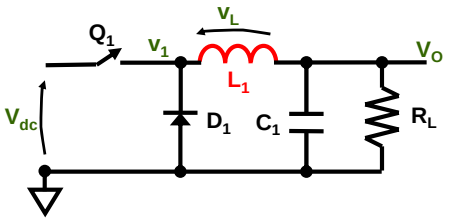




Let's discuss the design of the inductor. The inductor stores energy in its magnetic field during T_{ON}, and releases it during T_{OFF} to supply a constant voltage to the output load. Along with the capacitor, it also operates as an LC filter which filters out the current ripple.

Buck Converter Design – Inductor

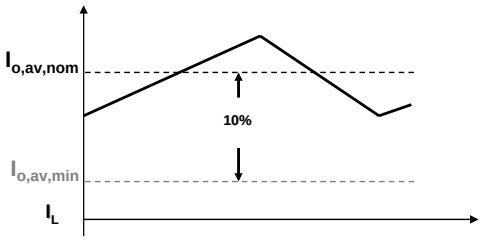
$$I_{o,av,\min} = 0.1 I_{o,av,nom}$$



$$I_{o,av,\min} = 0.1 I_{o,av,nom} = \frac{(V_{dc,nom} - V_o)}{2L_1} T_{on}$$

Solving

$$L_1 = \frac{5(V_{dc,nom} - V_o)V_o}{V_{dc,nom} F_{PWM} I_{o,av,nom}}$$



The inductor design equation can be obtained considering the minimum output current that the converter must be able to supply.We know that the average inductor current is also the load current. If we want the converter to operate in continuous mode only, the minimum output current should be greater than zero at the beginning and the end of each period.

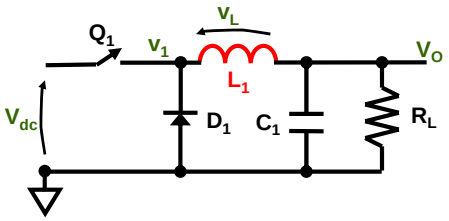
Buck Converter Design – Inductor

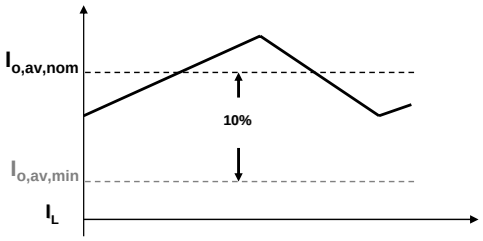
$$I_{o,av,\min} = 0.1 I_{o,av,nom}$$

$$I_{o,av,\min} = 0.1 I_{o,av,nom} = \frac{(V_{dc,nom} - V_o)}{2L_1} T_{on}$$

Solving

$$L_1 = \frac{5(V_{dc,nom} - V_o)V_o}{V_{dc,nom} F_{PWM} I_{o,av,nom}}$$





We can then define the minimum output current as one tenth of the nominal output current .

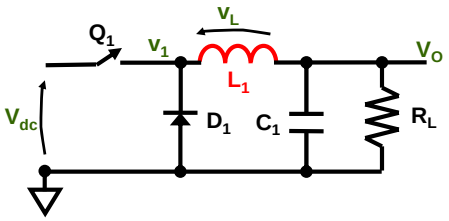
Buck Converter Design – Inductor

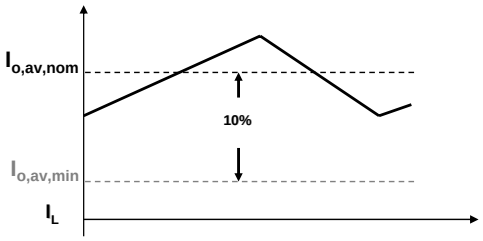
$$I_{o,av,\min} = 0.1 I_{o,av,nom}$$

$$I_{o,av,\min} = 0.1 I_{o,av,nom} = \frac{(V_{dc,nom} - V_o)}{2L_1} T_{on}$$

Solving

$$L_1 = \frac{5(V_{dc,nom} - V_o)V_o}{V_{dc,nom} F_{PWM} I_{o,av,nom}}$$

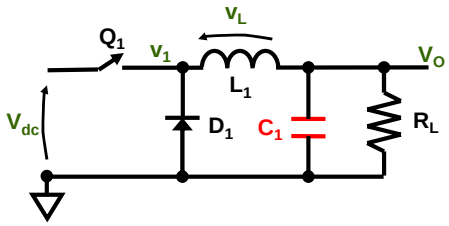




By using the equation for current flowing through the inductor during $T_{ON,}$ we can obtain the value of the inductor.

As seen in the design equation, the pwm frequency (F_{PWM}) appears in the denominator. Therefore, increasing the switching frequency will allow for smaller components, both in terms value an in size. There is thus a trend in buck converter design to use as high a PWM frequency as possible. At the same time, increase in frequency the dissipation in the switching elements due to switching losses thus reducing the overall efficiency. The typical frequency range of F_{PWM} is between 100 and 500 kHz.

Buck Converter Design – Output Capacitor

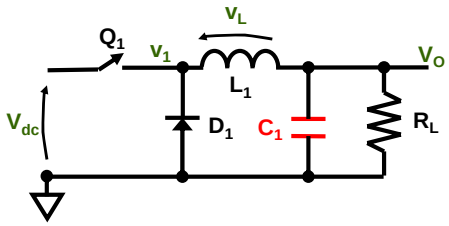


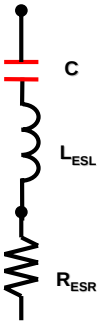
$$C_0 = \frac{\Delta I_L D}{F_{PWM}\left[\Delta V_{r,total} - R_{ESR}\Delta I_L\right]}$$

Let's discuss the design of the output capacitor.

The selection of the output capacitor is essentially related to the need to guarantee a limited amount of ripple at the output. The current flowing through the inductor has a siginificant amount of ripple which must be filtered by the capacitor. Noting that the capacitor is not ideal,

Buck Converter Design – Output Capacitor





$$C_0 = \frac{\Delta I_L D}{F_{PWM}\left[\Delta V_{r,total} - R_{ESR}\Delta I_L\right]}$$

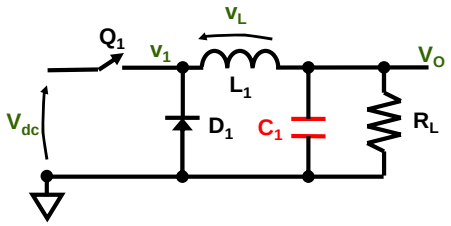
we replace it by its equivalent circuit, which is a series connection of an “ideal” capacitor, a resistor (R_{ESR}) and an inductor (L_{ESL}). The total output voltage ripple on the capacitor must not be bigger than the maximum allowable output ripple. In the computation of the output voltage across the capacitor, the load resistance, although it is small, is much bigger than the series resistance of the capacitor model and can be neglected. The inductance term is neglected for simplicity.

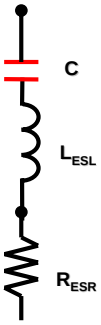
The voltage ripple contribution comes from two terms:

1. The voltage drop across R_{ESR} generated by the current. Its value can be computed considering the current ripple.
2. The voltage drop across the “ideal” capacitor as from the basic equation.

As stated, the summation of these two contributions must be equal or less than the maximum allowable output ripple voltage, delta $V_{r,total.}$

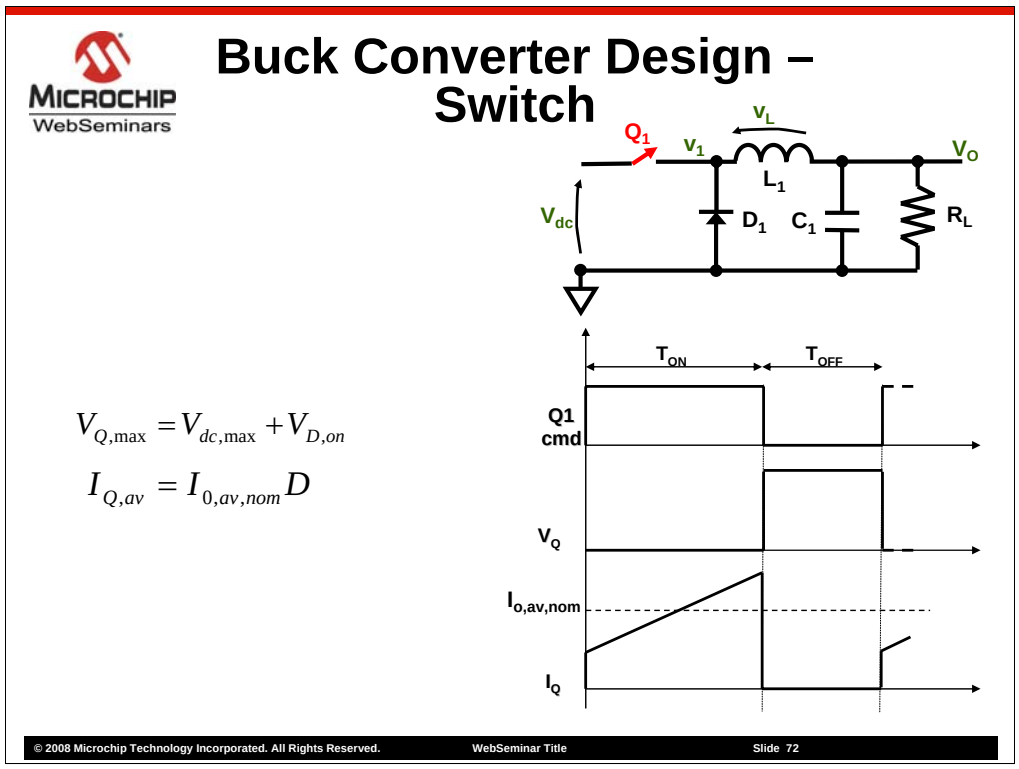
Buck Converter Design – Output Capacitor





$$C_0 = \frac{\Delta I_L D}{F_{PWM}\left[\Delta V_{r,total} - R_{ESR}\Delta I_L\right]}$$

Summing and rearranging terms, we get the capacitor value.

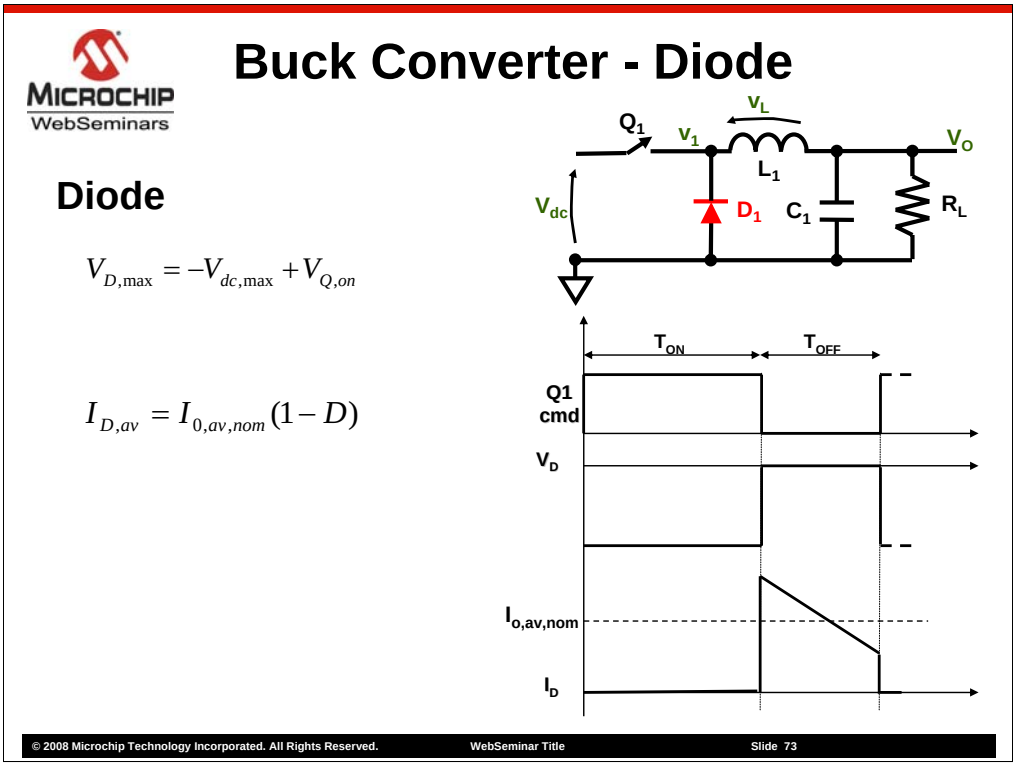


Switch Q1 is usually a MOSFET device. The basic requirement is that the MOSFET must be able to withstand the maximum voltage and current that it will experience during the operation of the circuit.

As seen in the diagram, these values occur during T_{ON} and T_{OFF}.

1. During T_{ON} the voltage across Q1 is near zero, the current is the same current flowing into the inductor and it has a linear up-slope behavior.
2. During T_{OFF} the voltage across Q1 is at its maximum (close to V_{dc}) and the current is zero.

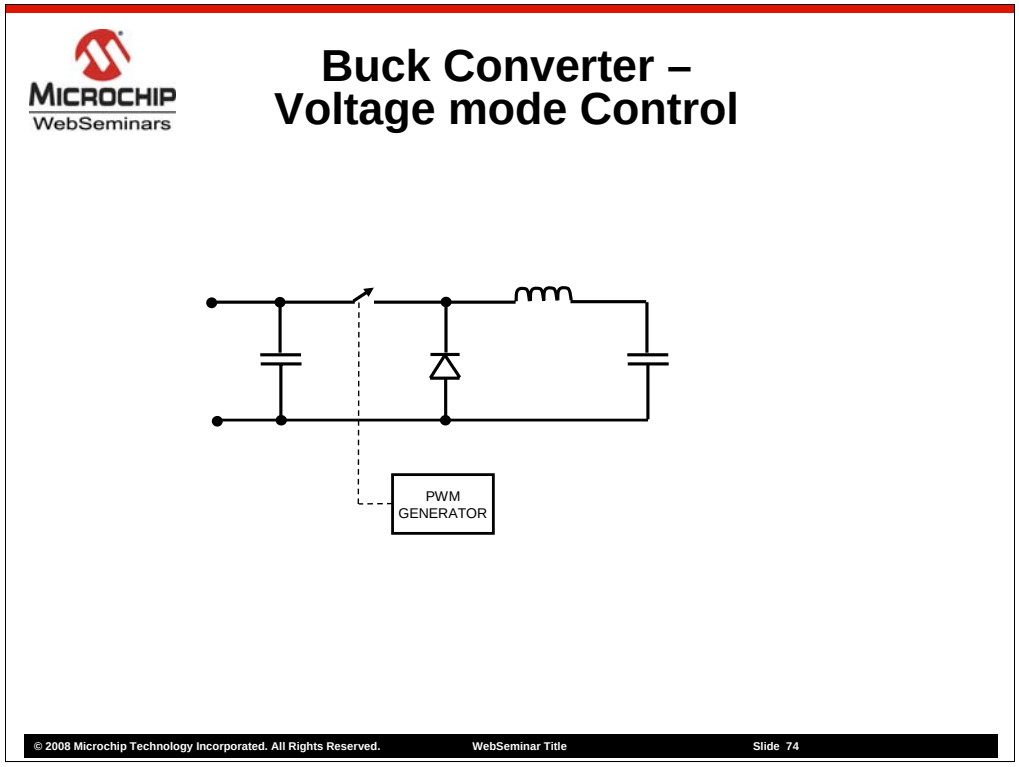
Consequently, the maximum voltage that the MOSFET must sustain is the maximum input voltage ($V_{dc,max}$), which is a design specification. It must comfortably handle the nominal output current (which is again a design specification).



A similar analysis is performed on the freewheeling diode. We consider the maximum voltage and (average) current this diode must handle.

1. During T_{ON} the voltage is close to $-V_{dc}$ and the current is zero (the diode is open). Therefore, the maximum reverse voltage across the inductor would be $V_{dc,ma}$
2. During T_{OFF} the voltage across the diode is close to zero (diode forward voltage), but the current through it is the same as the current flowing into the inductor and the output ($I_{o,av,nom}$).

These values can be used to select the diode.

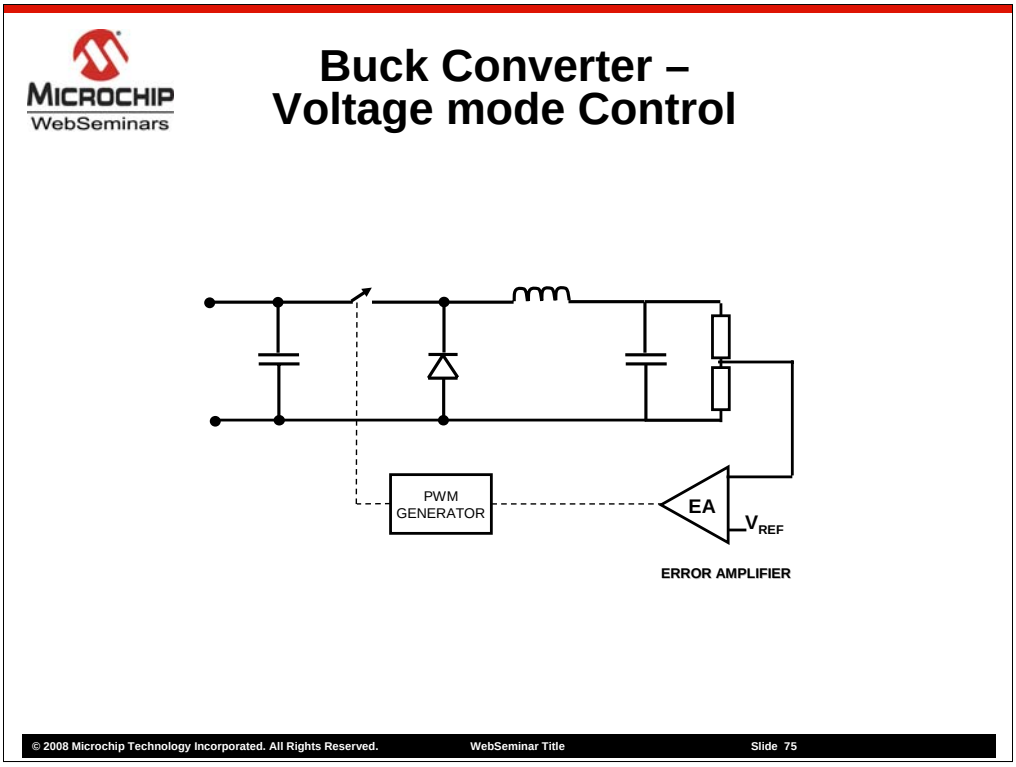


We will now discuss techniques to maintan a stable output voltage in the buck converter. In the design process of a buck converter the input voltage and the output voltage are the known quantities. The system must use the correct duty cycle to ensure that the desired output voltage is obtained using the available input voltage. In an ideal situation, the output and input voltage would not change during system operation and the duty cycle could be kept constant.

However in reality there are a number of reasons why the system performance may degrade:

1. The input voltage can vary with in a wide range.
2. The input voltage can have glitches, spikes, and noise.
3. The outpout load can vary e.g. when connecting/disconnnecting loads.
4. Presence of Noise.
5. And variations due to temperature, components tolerances, and aging.

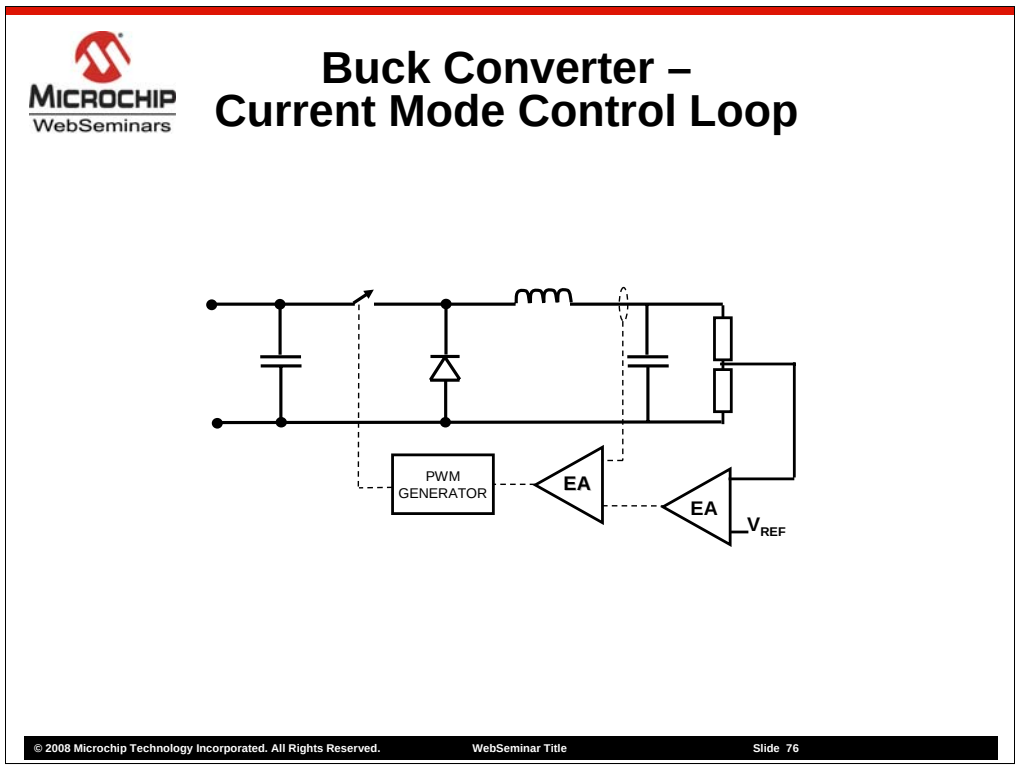
If there is no mechanism to prevent the output voltage from changing, the system could misbehave and may not produce a stable output.



To prevent this, a closed loop system is used. In a closed loop system, the output voltage is continuously monitored, and a corrective action is performed in case the output voltage shifts from it's intended value. The end result of the corrective action is a change in the duty cycle of the signal driving the MOSFET.

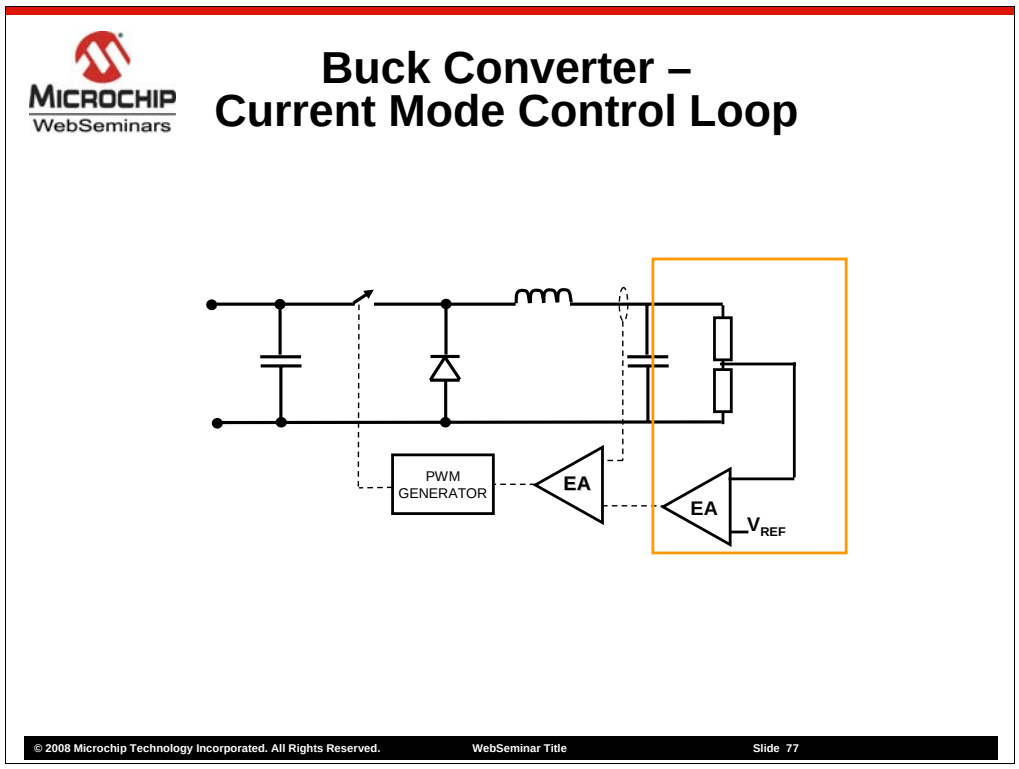
There are basically two approaches that can be used to implement a closed loop system for the buck converter. In the "voltage mode control" approach, the output voltage is monitored and compared to a reference value. The difference, which is the error, is then processed by an error amplifier. The final steps are to modify the PWM duty cycle to correct the output volatge.

The challenge in designing such a system is to make the control loop stable. The transfer function of the error amplifier should be such that the whole system is unconditionally stable.

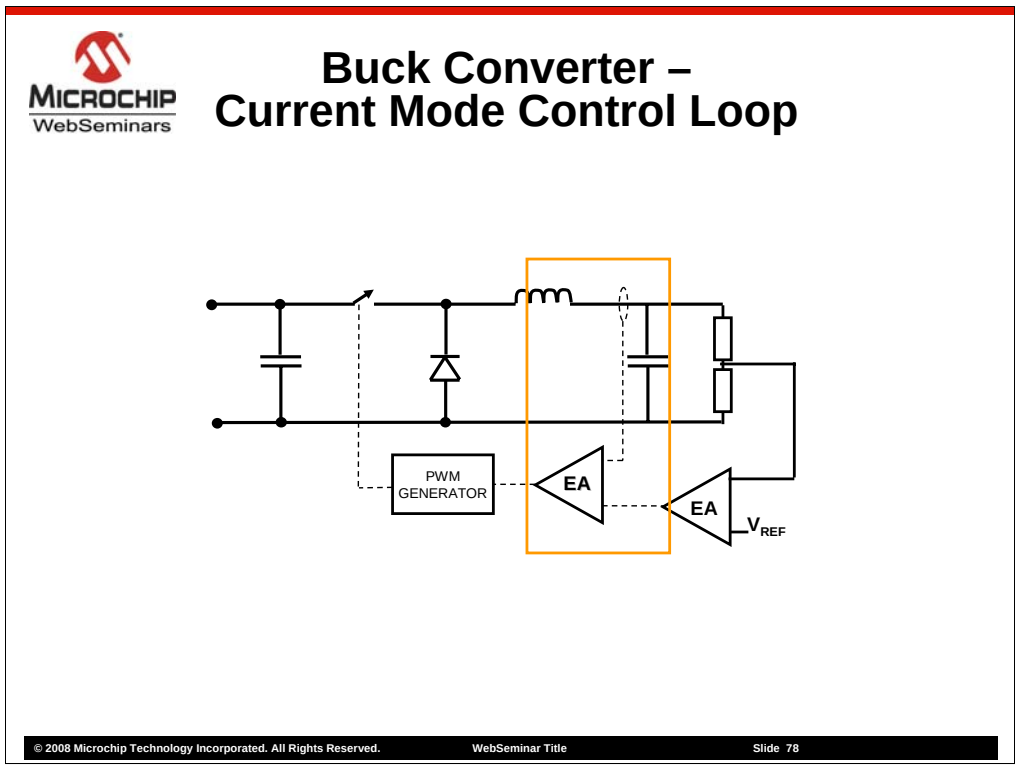


Another approach to implementing a control loop with a buck converter is called Current Mode Control.

This mode is actually made up of two loops:

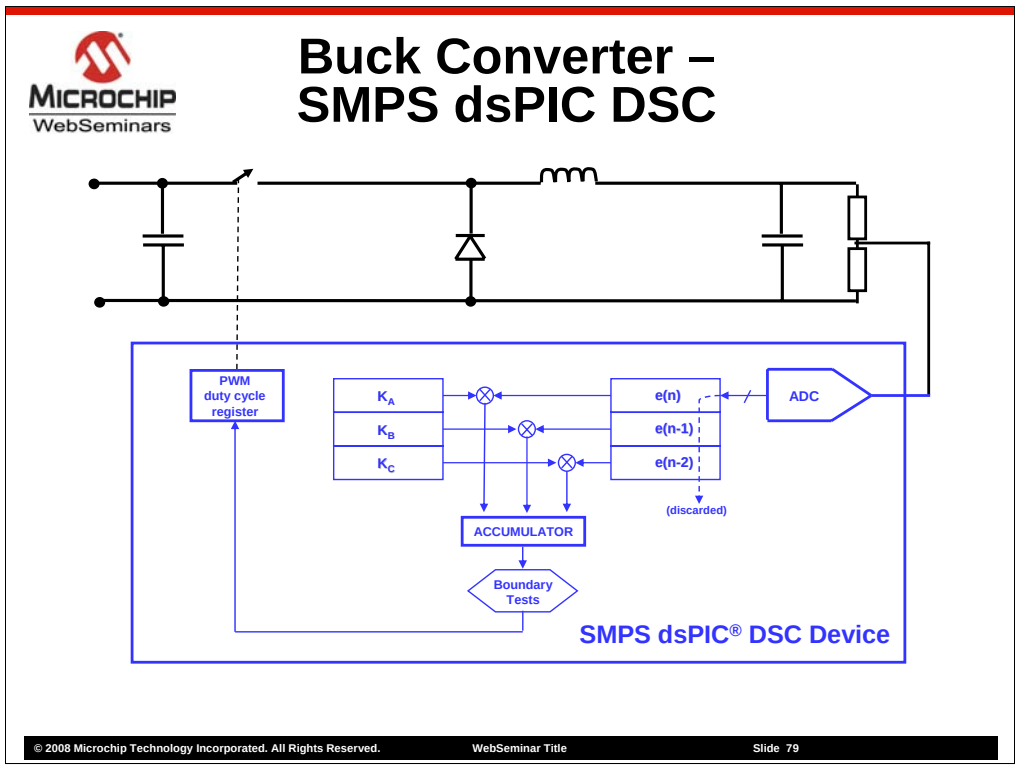


1. The external one, which is a voltage loop (which is the same as the one described previously)



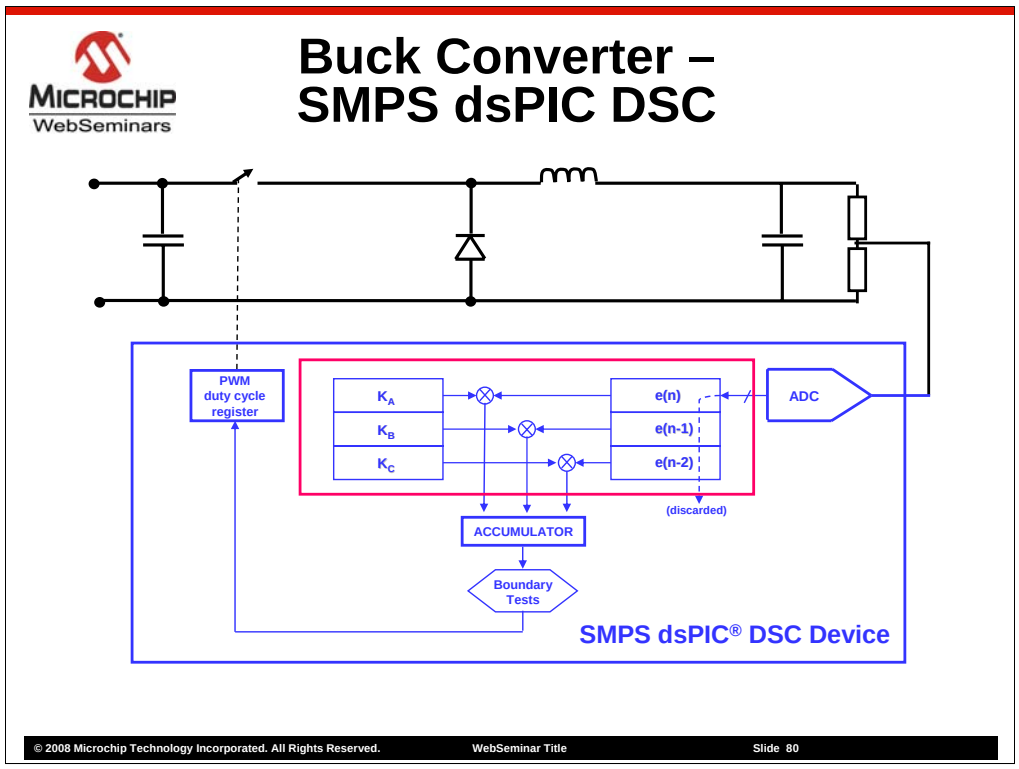
2. And an inner loop, which is the current loop.

The basic idea in current mode control is to operate directly on the variable that is responsible for the output behavior. In this case this variable is the inductor current. If the input or output voltages change, the inductor current has to change correspondingly in order to maintain a constant output voltage. Reading the current and making the system respond to its variation, also makes the overall system much faster in responding to transients.

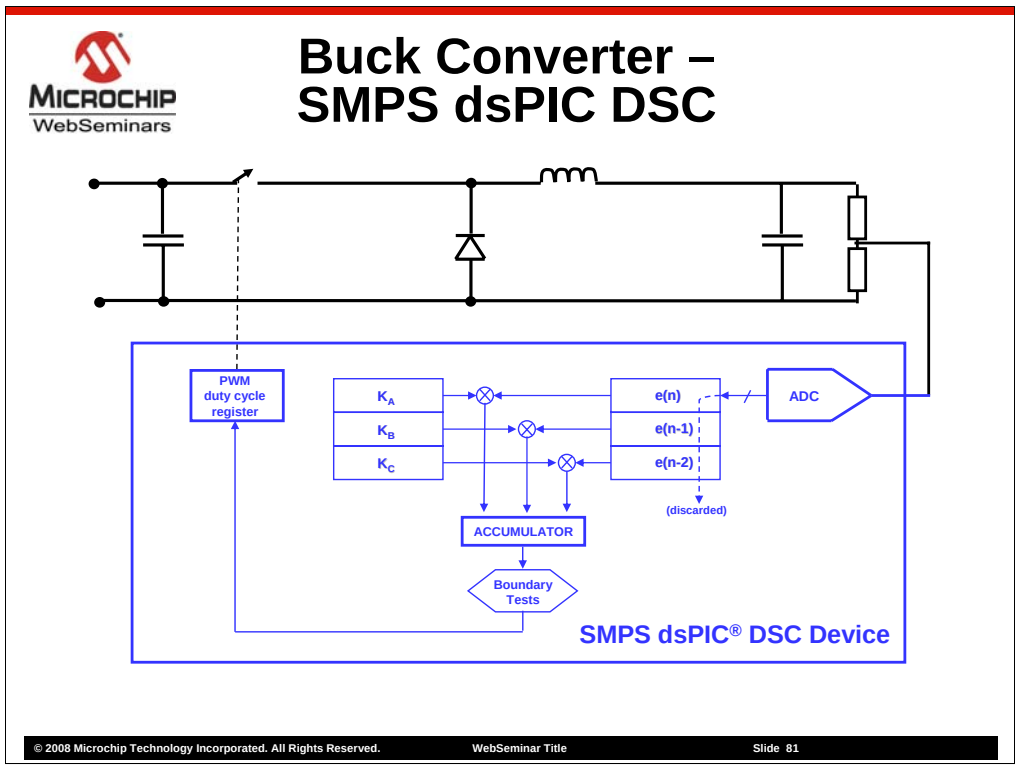


Here we see an example of basic voltage mode control loop using Microchip's SMPS dsPIC DSC devices. This digital implementation differs from the "traditional analog" implementation in two respects:

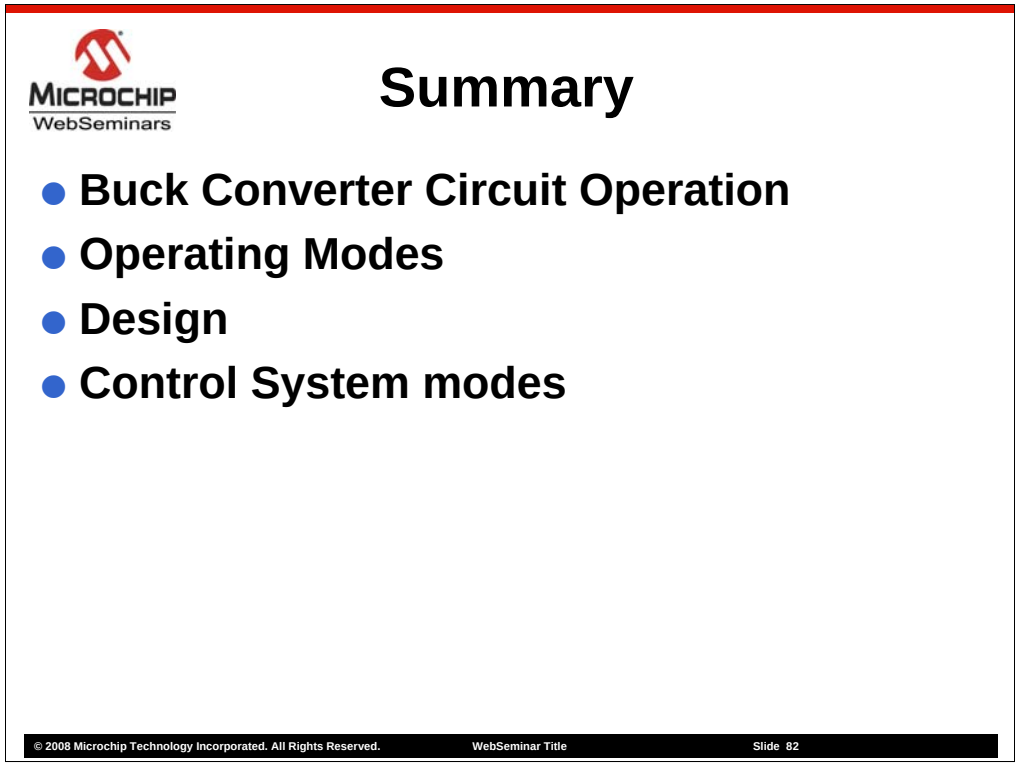
1. The output voltage (and current also in a current mode loop) is converted to digital values using the Analog-to-Digital converter.
2. The Error Amplifier is replaced by the digital implementation of a proportional-integral-differential or the PID controller.



The slide shows the basic function performed by the PID controller. It computes a corrective action based on the sum of of three products between errors and some coefficients K_A, K_B and K_C. The errors that are used in this implementation are the current error value, the previous error value, and the error value that is two sampling periods old. The SMPS dsPIC DSC device has a powerful DSP engine that allows a fast and precise computation of the new value of the duty cycle.



Along with the PID controller, some additional functions have to be added for a real world design. These include functions such as fault management for conditions such as overcurrent and overtemperature, sequencing, and input voltage monitoring; All of these functions can be performed by the specialized peripherals in the dsPIC DSC device. Changing the behavior of the control loop will require only changes in the dsPIC DSC firmware without any changes to the hardware



In summary

1. The basic operation of the buck converter was discussed and a steady state analysis was performed.
2. The Continuous, Critical and Discontinuous operating modes were discussed.
3. We looked at the design consideration of the individual components of the buck converter.
4. We finally discussed the voltage mode and current mode control methods and the use of feedback control systems.

This brings us to the end of this webinar.