

Industrial Flyback with TPS40210 and universal transformer

- 9 ... 36V input, 5.0V @ 4.0A output
- Flyback with synchronous rectification for maximum efficiency
- Transformer can be used for 5.0V @ 4.0A or 12.0V @ 1.5A
- Built on PCB PMP4626 Rev. E

1 Startup

The startup waveform is shown in Figure 1.

The input voltage is set at 24.0V, with no load on the output.

Channel C1: **input voltage**
5V/div, 2ms/div

Channel C2: **output voltage**
2V/div, 2ms/div

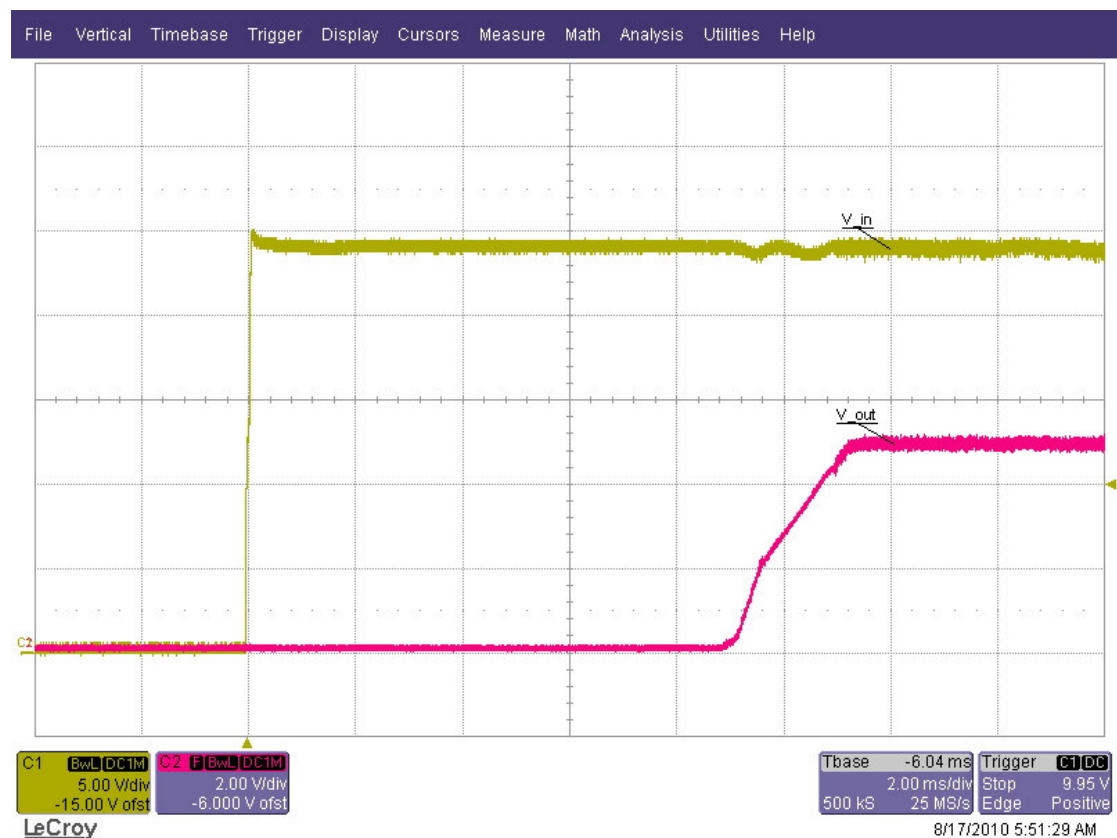


Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2.
The input voltage is set at 24.0V with a 4.0A load on the output.

- Channel C1: **input voltage**
5V/div, 500us/div
- Channel C2: **output voltage**
2V/div, 500us/div

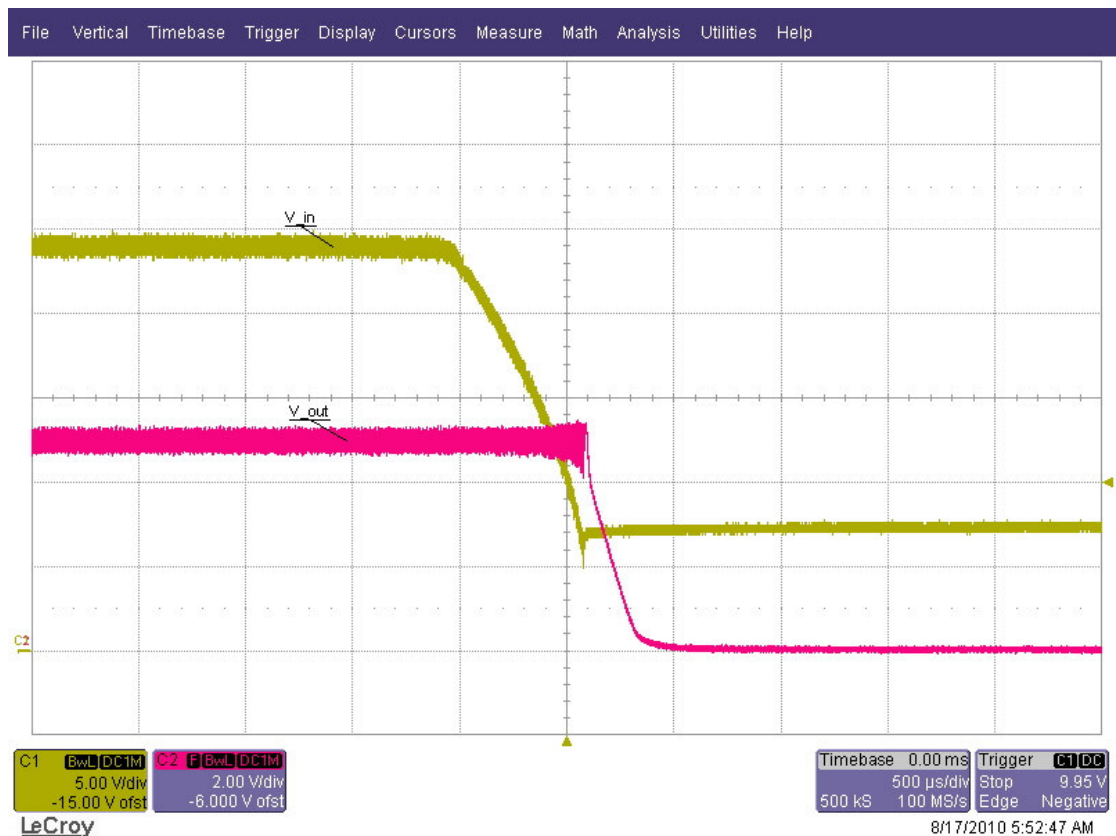


Figure 2

3 Efficiency

The efficiency of the converter is shown in Figure 3.

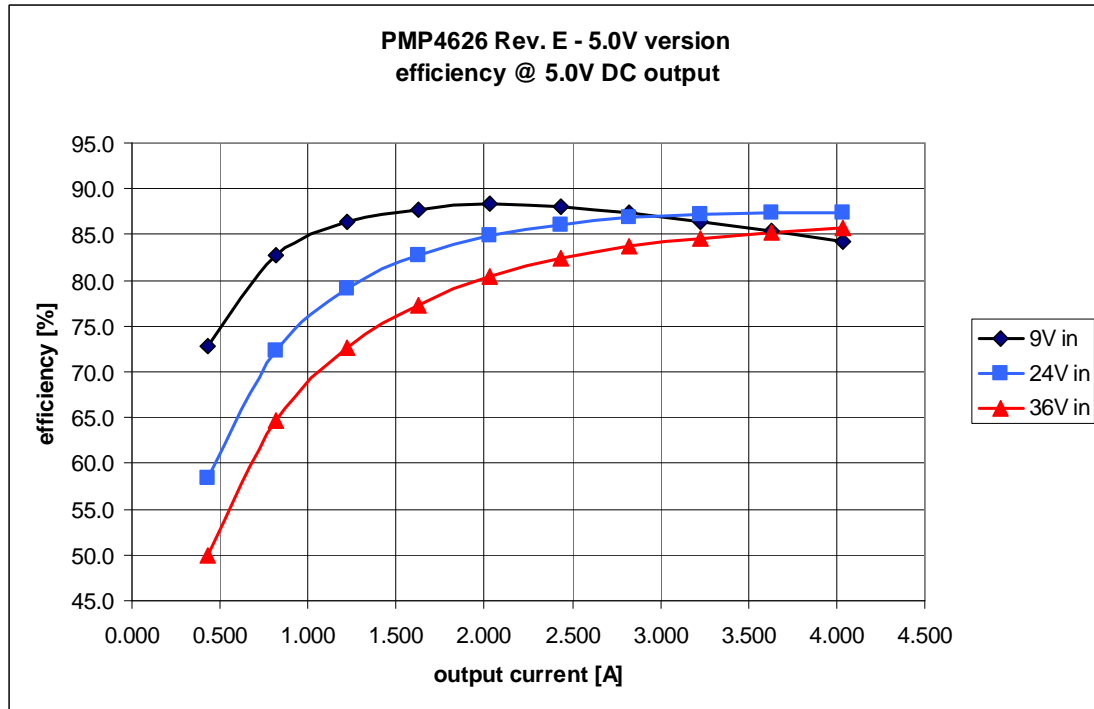


Figure 3

4 Load regulation

The load regulation is shown in Figure 4.

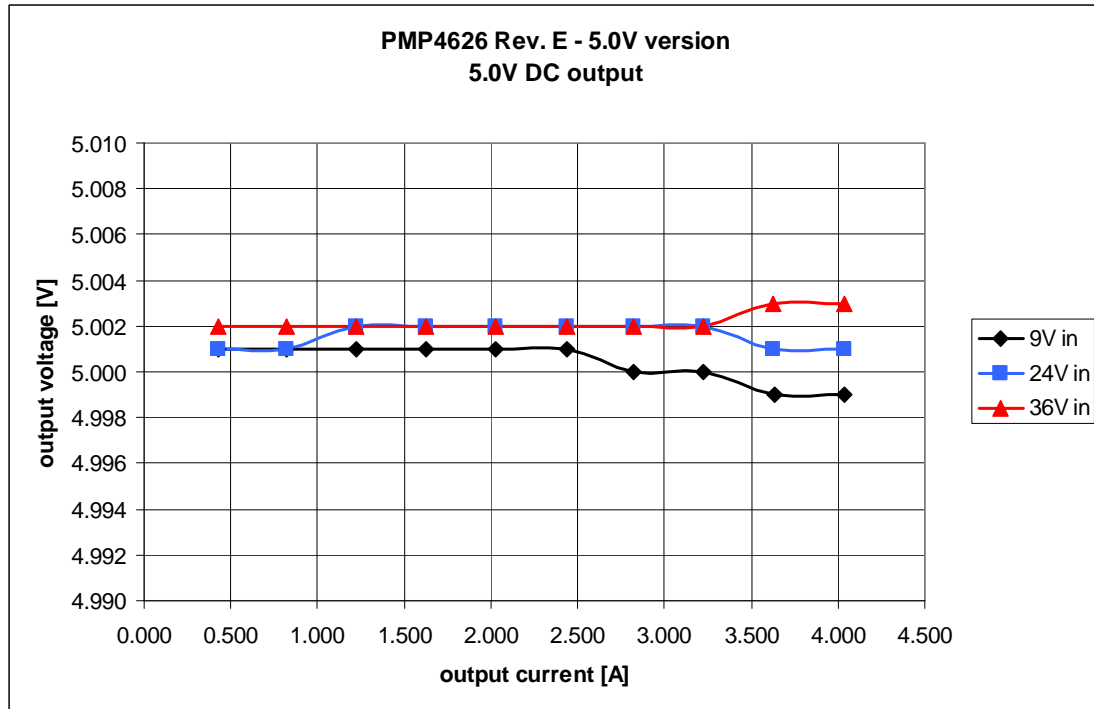


Figure 4

5 Output ripple voltage

The output ripple voltage at 4.0A load and 9.0V, 24.0V and 36.0V input voltage is shown in Figure 5.

Channel M1: **output voltage, 50mV peak-peak, 9.0V in**
50mV/div, 5us/div, AC coupled

Channel M2: **output voltage, 40mV peak-peak, 24.0V in**
50mV/div, 5us/div, AC coupled

Channel M3: **output voltage, 30mV peak-peak, 36.0V in**
50mV/div, 5us/div, AC coupled

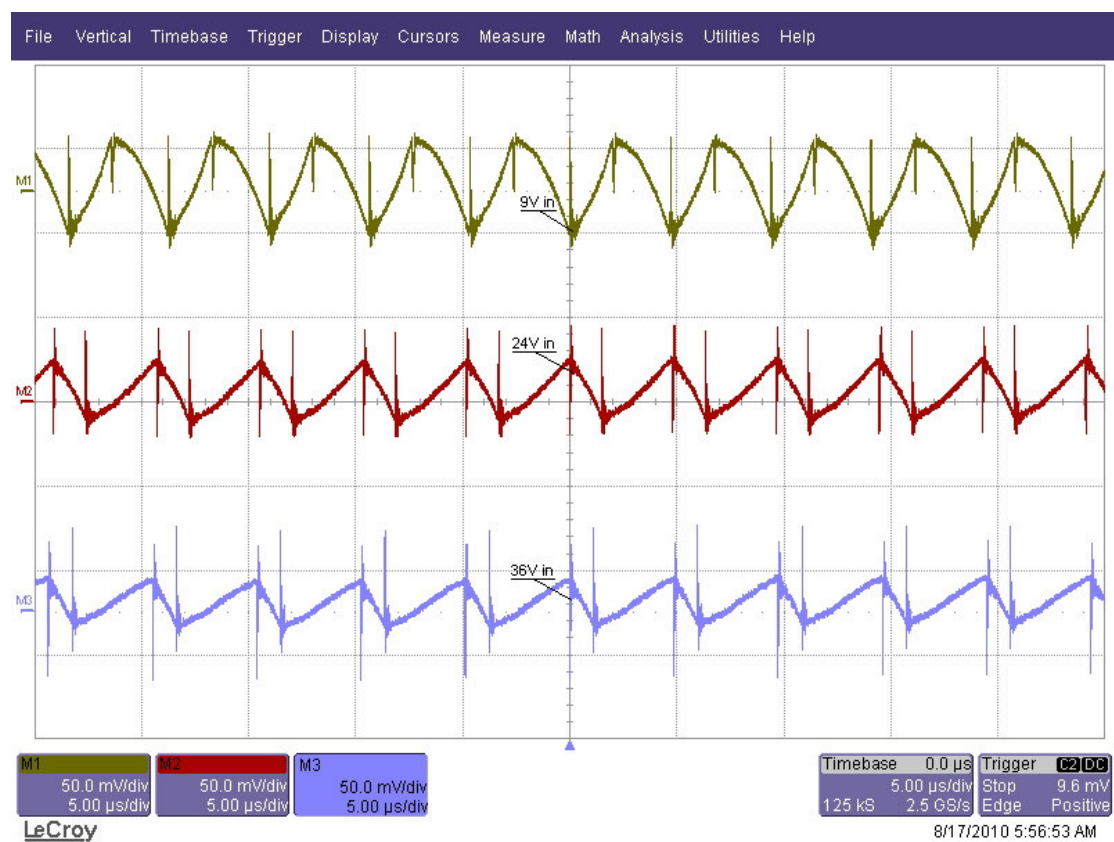


Figure 5

6 Load transients

The response to a load step and a load dump at an input voltage of 24.0V is shown in Figure 6 and Figure 7.

Channel C2: **output voltage**, -380mV undershoot, 90mV overshoot
200mV/div, 100us/div, AC coupled

Channel C1: **load current**, load step 2.0A to 4.0A
2A/div, 100us/div

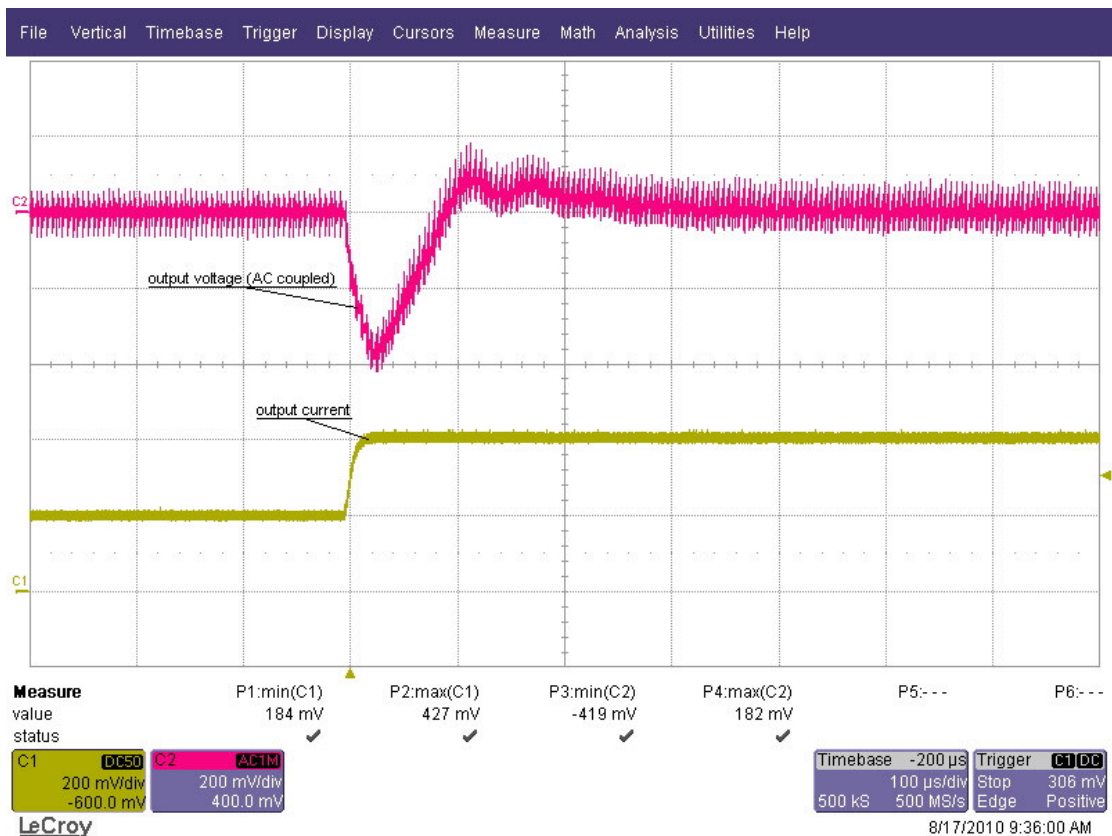


Figure 6

Channel C2: **output voltage**, 360mV overshoot, -80mV undershoot
 200mV/div, 100us/div, AC coupled

Channel C1: **load current**, load dump 4.0A to 2.0A
 2A/div, 100us/div

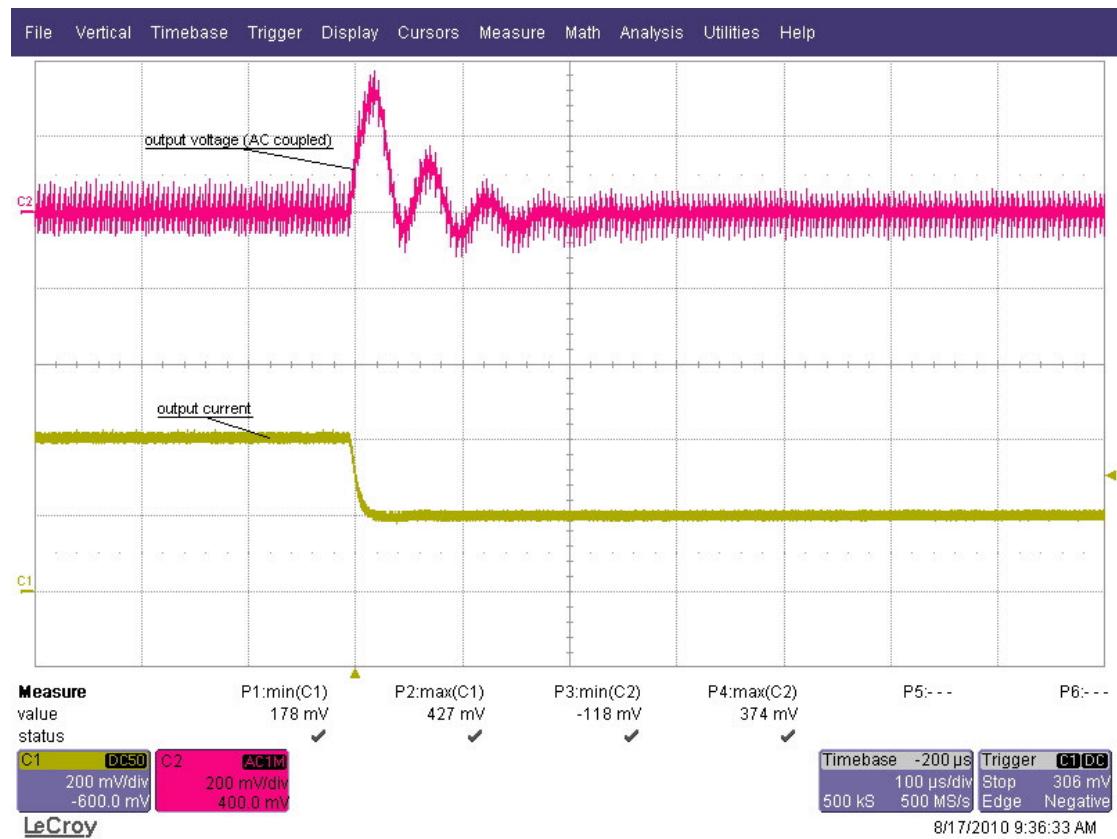


Figure 7

7 Frequency response

Figure 8 shows the loop response with 9.0V, 24.0V and 36.0V input with a 4.0A load on the output.

- 80 deg phase margin @ crossover frequency 1.20 kHz with 9.0V input voltage
- 85 deg phase margin @ crossover frequency 1.15 kHz with 24.0V input voltage
- 85 deg phase margin @ crossover frequency 1.14 kHz with 36.0V input voltage

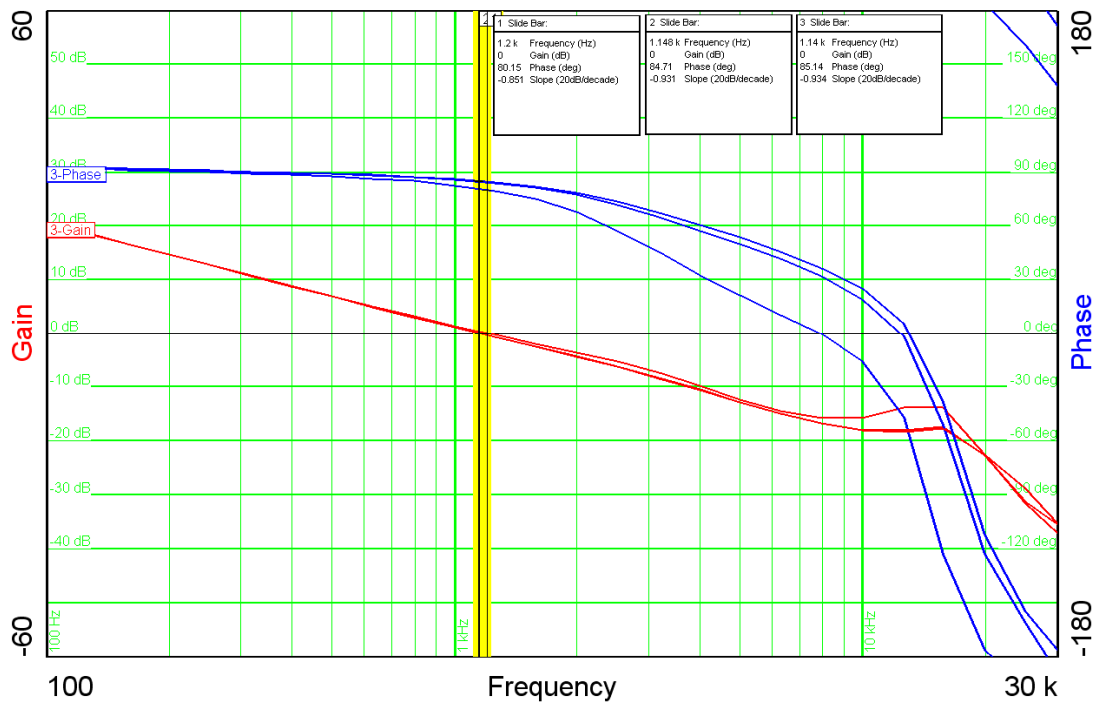


Figure 8

8 Miscellaneous waveforms

The voltage on the switching node (Q3, primary side) is shown in Figure 9.
The image was captured with a 36.0V input and a 4.0A load.

Channel C2: **switching node voltage**, -2.6V minimum voltage, 62.3V maximum voltage
10V/div, 2us/div

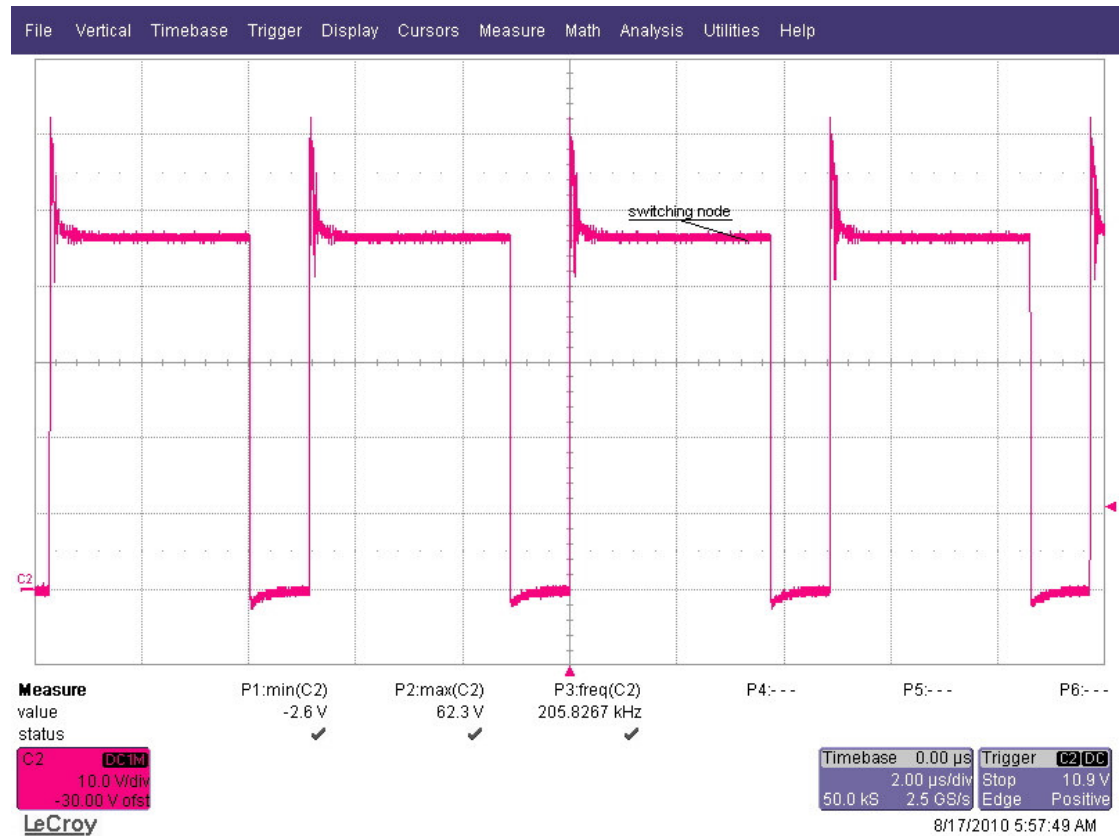


Figure 9

The drain-source voltage of the secondary side FET for rectification is shown in Figure 10. The image was captured with a 36.0V input and a 4.0A load.

Channel C2: **drain-source voltage**, -2.3V minimum voltage, 44.1V maximum voltage
10V/div, 2us/div

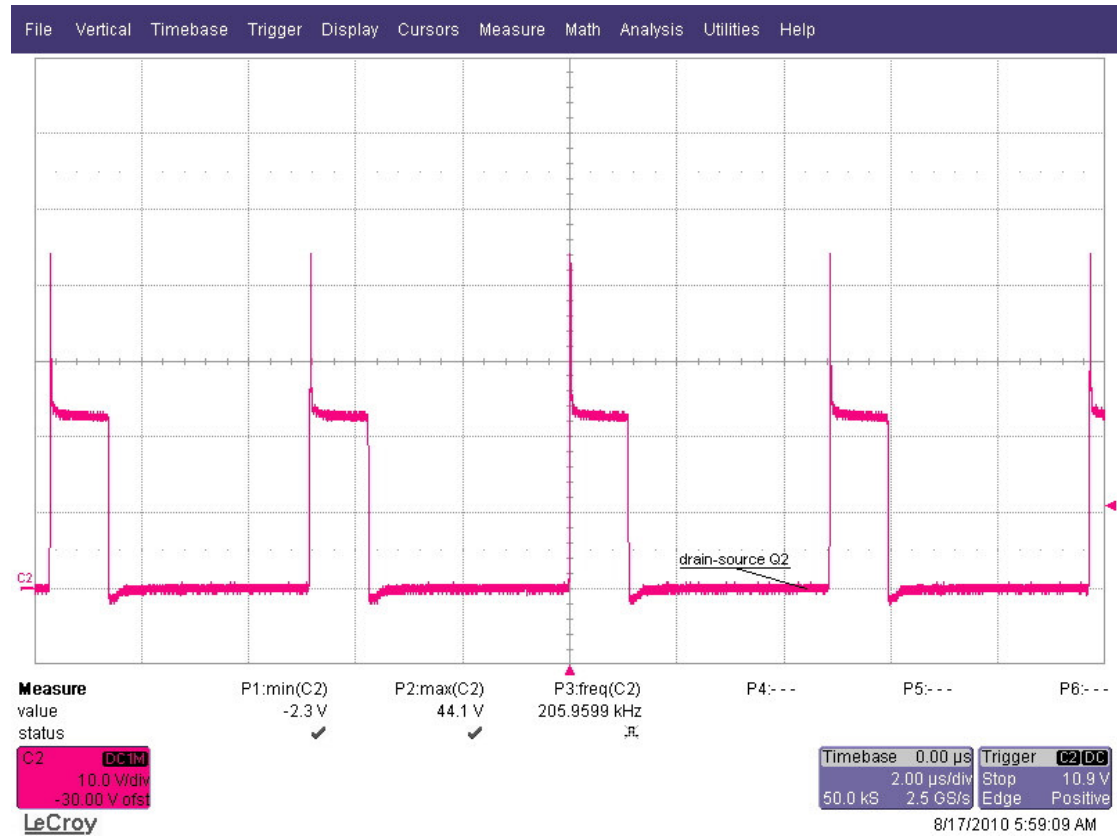


Figure 10

The gate-source voltage of the secondary side FET for rectification is shown in Figure 11. The image was captured with a 36.0V input and a 4.0A load.

Channel C2: **gate-source voltage**, -18.4V minimum voltage, 5.9V maximum voltage
5V/div, 2us/div

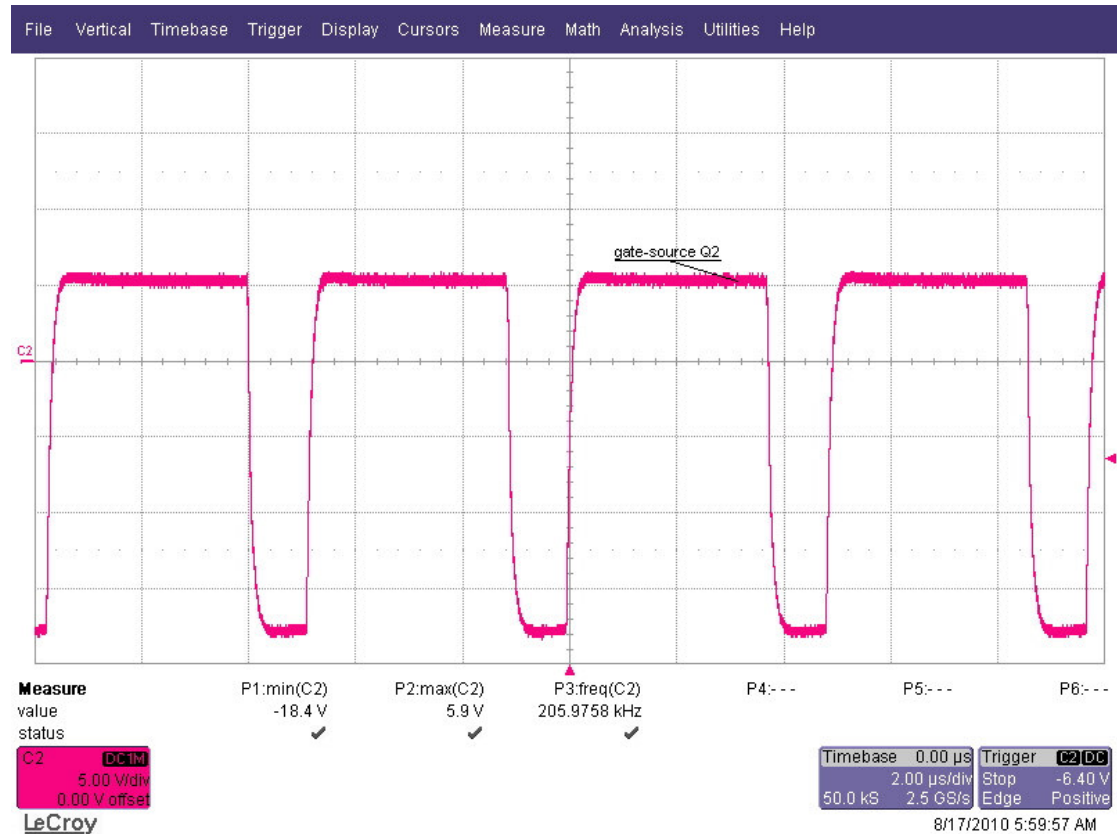


Figure 11

9 Thermal measurement

The thermal image (Figure 12) shows the circuit at an ambient temperature of 25 °C with an input voltage of 9.0V and a load of 4.0A.

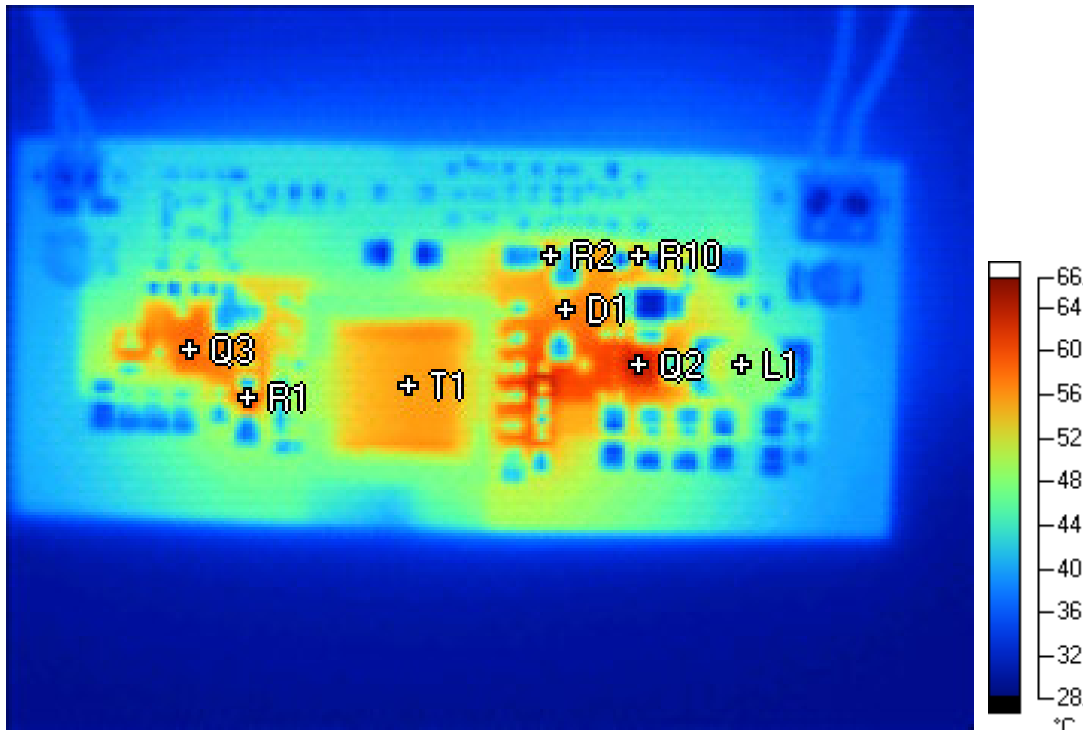


Figure 12

Label	Temperature
Q3	58.3 °C
R1	59.4 °C
T1	55.3 °C
R2	59.1 °C
D1	57.0 °C
R10	56.6 °C
Q2	63.5 °C
L1	48.1 °C

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