Lecture 14
Disadvantages of Transformers and Introduction to the Flyback Converter

I. Use of Transformers or Coupled Inductors in PWM Converters

A. Disadvantages of Transformers for PWM Converter Circuits

II. Flyback Converter with a Coupled Inductor Transformer Drive

A. Origin of the flyback from the buck-boost
B. Circuit Model for CCM and DCM Operation
C. Erickson Problem 6.4: Two Transistor Flyback Implementation in DCM Operation

III. Flyback Converter Mode Transformer

LECTURE 14

Use of Transformers or Coupled Inductors in PWM Converters

I. Disadvantages of Transformers in PWM Circuits

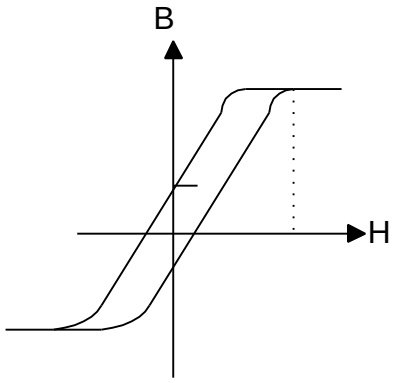
We list below **four disadvantages** to the use of transformers, operating at f_{SW}, in PWM converter circuits.

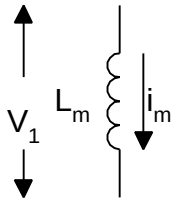
1. Step-up/down voltages, that now vary over a wider dynamic range due to transformer action, may further stress solid state components in either the current through the switches or the voltages across them. Due to the presence of magnetic storage elements we will also see larger peak values of switch stress caused by, for example, **leakage / parasitic inductance's**.

2. **Inadvertent net V_L DC levels**, even very small ones, across inductors or transformers may lead to saturation of the cores as time evolves and we go through many switch cycles. That is, even though the net V_L is small we quickly add up the offset via the large number of switch cycles involved.

$\int v_L(dc)\,dt \Rightarrow i_L \rightarrow \infty$ because the inductance ,L, is sharply reduced when the core saturates we give a large sometimes **fatal stress to the series switch** due to the low impedance paths suddenly available.

On the following page we show the non-linear B-H curve that gives rise to sudden changes in the permeability when H goes above $H_{critical}$ or I_L exceeds the critical current.





$$V_1 = L_m \frac{di_m}{dt}$$

Consider a time interval T_{sw}

$$i_m = \frac{\int_0^{T_s} V_1 \, dt}{L} = i_m(T_s) - i_m(0)$$

In steady state i_m should not have a net increase over the duration T_s. That is the time average of V_L should be zero. Otherwise current i_m will grow without bound due to core saturation every switch cycle till we reach saturation.

3. Losses in either transformer cores or inductor cores

a) Hysteresis $P_{loss} \sim f$. This arises from magnetic poles in the core material being aligned and then reversed each half switching cycle for bipolar drives. The loss is proportional to the frequency of the flux

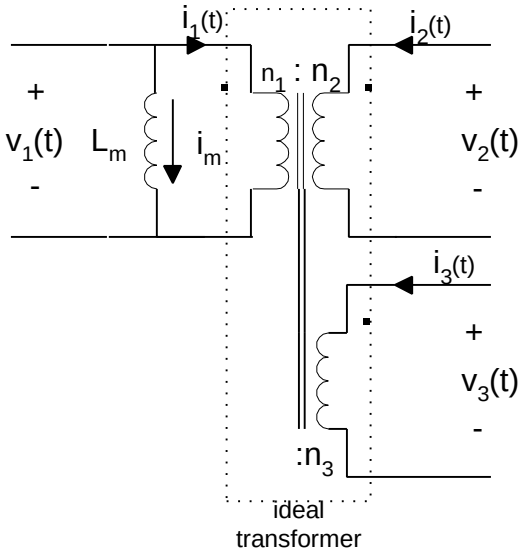
b) Eddy currents $P_{loss} \sim f^2$. This current in the magnetic core material arises because: the current in the copper wire at f_{sw}

will induce a time varying flux at f in the magnetic core. In turn the time varying core magnetic flux induces by Faraday's Law a core electric field that drives an eddy current within the core material itself. This eddy current passes through the electrically resistive core material causing i^2R(core) losses. Overall, the core current induced will vary with $(f_{sw})^2$ as we will see in Erickson Chapters 12-13 at the end of first semester.

Often at low f_{SW} hystersis losses dominate and at high f_{SW} the eddy current losses dominate. Clearly, at some switch frequency the two loses are equal**. Such losses prevent f_{sw} from exceeding MHz frequencies** even though we want higher f_{SW}..

4. Complex Magnetizing Inductance Transformer Model and Current Flow Directions

Consider a three winding transformer with dots on one side of transformer to indicate similar phasing below:



We all know:

$$\frac{V_1}{n_1} = \frac{V_2}{n_2} = \frac{V_3}{n_3}$$

But we all may not know:
All i flow is assumed into dots in the formula below.

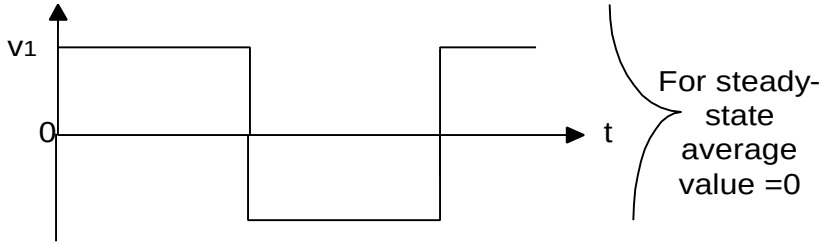
That is, note that current flow is assumed to flow into the dots in the transformer for establishing the conservation of mmf relationship:

$$n_1 i_1 + n_2 i_2 + n_3 i_3 = 0.$$

Any applied voltage $v_1(t)$ across L_m will cause a magnetizing current to flow: $i_m \equiv$ magnetizing current.

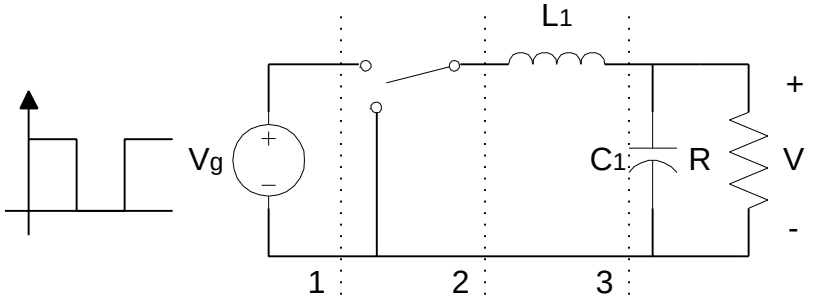
i_m will reach steady-state only provided that the average over T_s of V_1 is zero. Otherwise i_m will grow without bound.

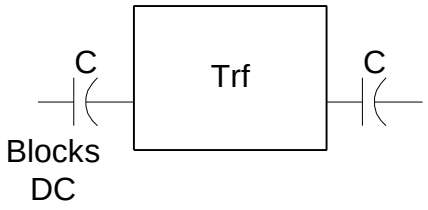
$$0 = \int_0^{Ts} V_1(t)\,dt$$



There is a precarious condition as we must deliver precisely $\pm V_L$. If there is a slight but fixed offset in the V_L cycle positive or negative then the magnetizing current will grow each T_s interval at a rate, f_{SW} until core saturation occurs.

This intolerance of even small offset voltages across inductors or transformer windings will limit where in the circuit topology one can "insert a transformer." In the circuit below 1 and 3 have dc voltages present - no transformer is ever allowed to be inserted there, unless we add a series capacitor to block any inadvertent DC offset voltage from appearing across the inductors.



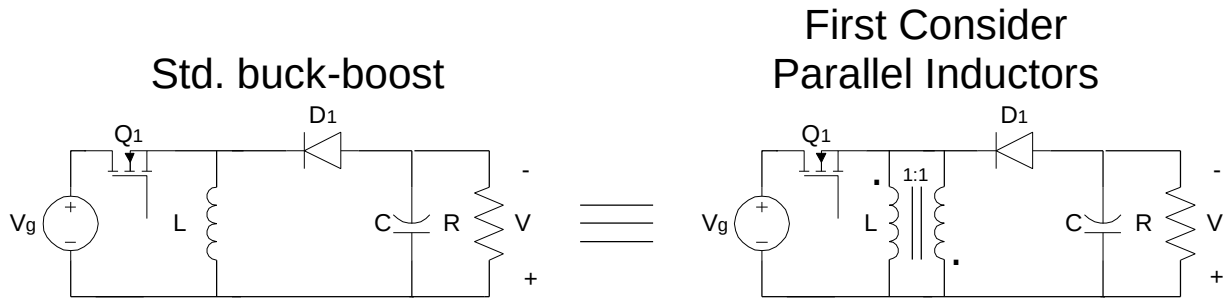


This series capacitor solution brings problems/changes to the low frequency gain of the converter loop gain. Also a series C may resonate with the parasitic leakage inductance of the transformer causing undesired oscillation.

Despite the above cautionary issues transformers are often employed in PWM circuits. To begin the use of transformers we will first look at the flyback converter, which as we will see is an isolated form of Buck-Boost.

II. Flyback Converter or Isolated Buck-Boost with a Coupled Inductor Transformer Drive

A. Origin from buck-boost



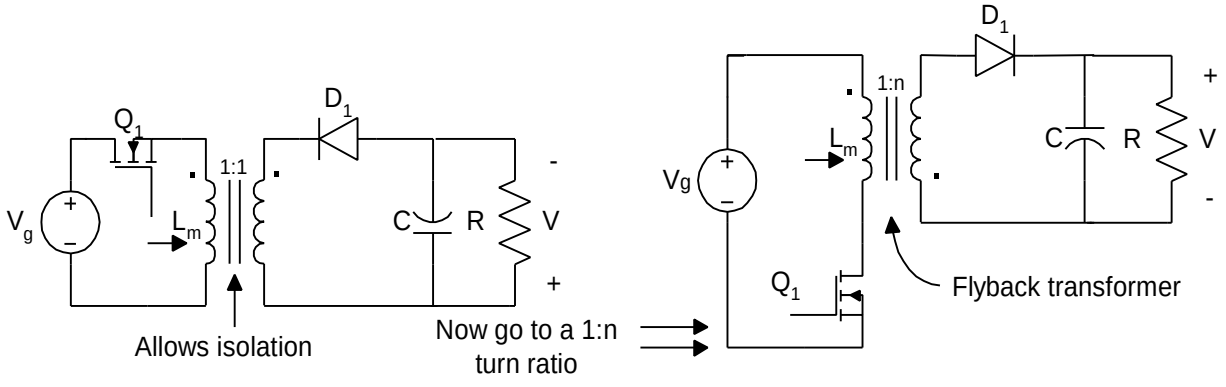
This simple coupled inductor still maintains the common ground connection that we may wish to avoid in many cases.

Flyback converters are employed for LOW POWER applications below 150 W and with voltages below 500V. Note that the core with an air gap doubles as a transformer and an output choke—**saving one heavy and costly component**.

Now cut the electrical connection between the two parallel inductors and **use only magnetic coupling between the two L's** by purposefully winding them on the same magnetic core. This makes for a <u>two winding</u> inductor--each separately wound and isolated electrically from each other except for the common magnetic core coupling . We now lose the common ground.

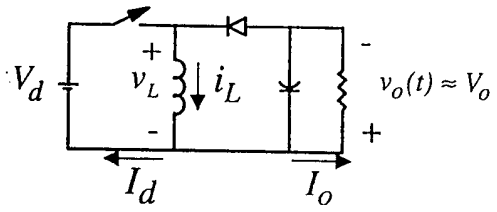
Current no longer flows simultaneously in the two electrically isolated inductor windings due to the core coupling alone because the primary and the secondary have their own series switches. Moreover, these switches can act in a complementary fashion so that when one is on the other is off.

When Q_1 is on for duration DT_s, i flows on left circuit into dot of L_m but no secondary current flows because diode D_1 blocks it with the dots shown. One must be careful to have transformer dots and diode directions both aligned to achieve this flyback action. When Q_1 is off then diode, D_1, is on for duration $D'T_s$, i flows on right half of circuit - this delayed secondary current is termed flyback current. Finally note the transformer can have any turns ratio. Note the way the dots and diodes are alternated in the two circuits below.



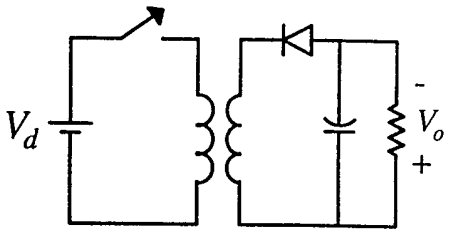
Flyback converter

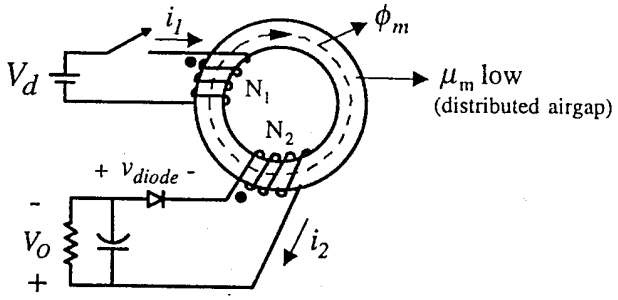
- Buck-boost topology



$$\frac{V_o}{V_d} = \frac{D}{1-D}$$

- needs L as a means of energy transfer
- two coupled coils





Note that the two copper wires are wound on the same magnetic core. **Not clearly shown is the fact that the core is purposely slotted to create an air gap**. This is unlike a transformer that has no air gap and hence stores no energy in the core. A transformer merely transfers energy from one coil to the other with no energy storage in the core. That is current flows SIMULTANEOUSLY in both copper wire windings in a transformer situation.

On the contrary in a flyback circuit, using an inductor coupling scheme, we do not have simultaneous current flow in both windings. Rather the large and purposeful air gap in the flyback core stores magnetic energy that we pump energy into the airgap during the transistor switch on cycle when current flows in the primary but not in the secondary. Next, the secondary winding removes this energy via secondary current flow but with no current

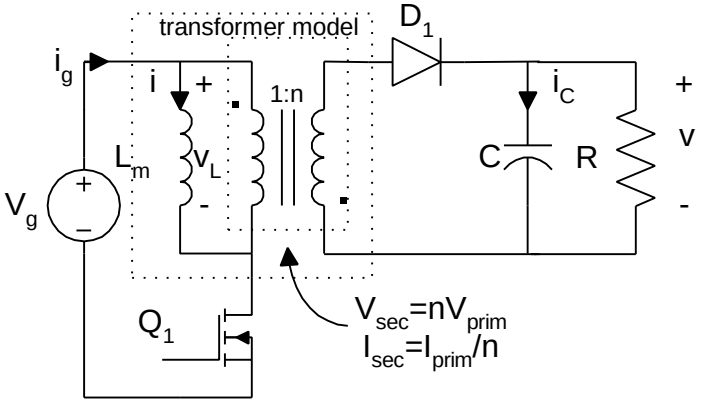
flow in the primary. This is flyback operation. Next we use the full transformer like circuit model to describe the coupled inductors and explain alternate current flows in the primary and secondary during different time intervals as well as energy storage.

B. Model of Flyback for CCM and DCM Operation

1) Magnetizing Inductance, L_m , Effects

In a flyback due to the air gap the core **reluctance is much larger** than in a core without an air gap. Hence, a **much smaller magnetizing inductance occurs** as compared to an un-gapped core where the magnetizing inductance is large. In short, in the flyback core L_M is small and a LARGE I_M current flows.

Use the circuit below for the analysis. The control signal switches Q_1 on then energy builds up in L_m for duration D_1T_s. Current is flowing into the L_m inductance but due to D_1 placement and the dot arrangement no secondary current flows.

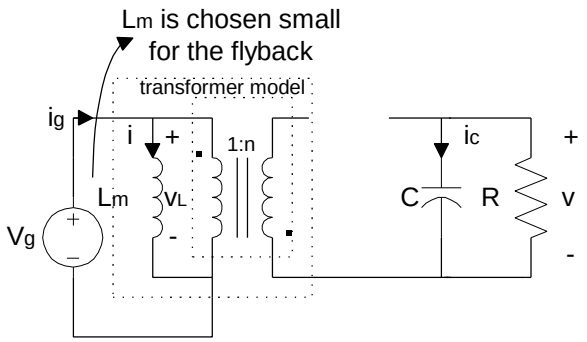


Assuming CCM, when the control voltage switches Q_1 off then i_{Lm} flows in a loop into the primary with one turn, n = 1, flowing out of the dot $\Rightarrow$ i flows in of the n-turn secondary winding as follows. It comes into the dot side of the secondary coil or out of the undot side of the coil turning D_1 on so that Σni = 0. L_m is chosen small to maximize i_m.

We repeat again, small L_m is achieved by cutting an air gap in the magnetic core to increase the core reluctance, $\mathcal{R}$, where:

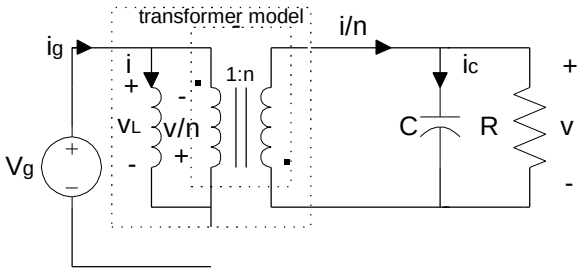
$L_m = \frac{mN^2}{\mathcal{R}}$. Hence L_M is much smaller than for a transformer.

D_1T_s



$V_{Lm} = V_p = V_G$ with Q_1 on
In the primary
All i flows through L_m.
$i_r + i_c = 0$ in the secondary.
As diode D_1 is off.

D_2T_s



With Q_1 off we find all i_m flows in n = 1 as a loop current coming out of the dot, in the primary and into the dot.

Note carefully that, only this choice of transformer current dots on the coils and diode placement on the secondary with the anode and cathode properly arranged causes the primary and secondary currents to alternate.

Note also that secondary current is 1/n of the primary current while primary voltage is 1/n of the secondary.

Hence: $i_c = -\frac{V}{R}$

In the secondary

$V_{Lm} = V_p = \frac{V_{sec}}{n} = -\frac{V_o}{n}$

$i_c = \frac{i}{n} - \frac{V}{R}$ This is the secondary flyback current flow.

Next we invoke our volt second balance to find the DC transfer function of the flyback converter.

For steady state to occur:

$$\langle v_{Lm} \rangle_{Ts} = 0, \quad D_1 V_g + D_2\left(\frac{-V_o}{n}\right) = 0$$

That is, if this equation is satisfied then the current in the inductor does not vary over many switch cycles. Hence we find the DC gain to be:

$$\frac{V_o}{V_g} = M(D) = \frac{nD_1}{D_2} = \frac{nD_1}{1-D_1} = \frac{nD}{D'}$$

Notice that the copper wire turns ratio, n, provides added flexibility to the V_o/V_g design.

Neglecting leakage inductance - the magnetic core doesn't matter.

$$\langle i_c \rangle = 0 \quad D_1\left(-\frac{V_o}{R}\right) + D_2\left[\frac{I}{n} - \frac{V}{R}\right] = 0$$

We can solve for the primary current I:

$$I = \frac{n V_o}{D_2 R}$$ or equivalently the secondary current $$\frac{I}{n} = \frac{V_o}{R}\,\frac{1}{D_2}$$

Again, the turns ratio, n, provides an additional way to hit the desired current beyond just varying the interval D_2.

Essentially, we can trade copper turns (n) on the coil for duty cycle (D) in the control circuits to vary the DC voltage and current gains.

Downside of ↑ n is added switch stress. Upside is we need less D to hit our target V_o.

Notice also for CCM operation with transformer winding dots properly placed by proper wire loops and diode placement right:

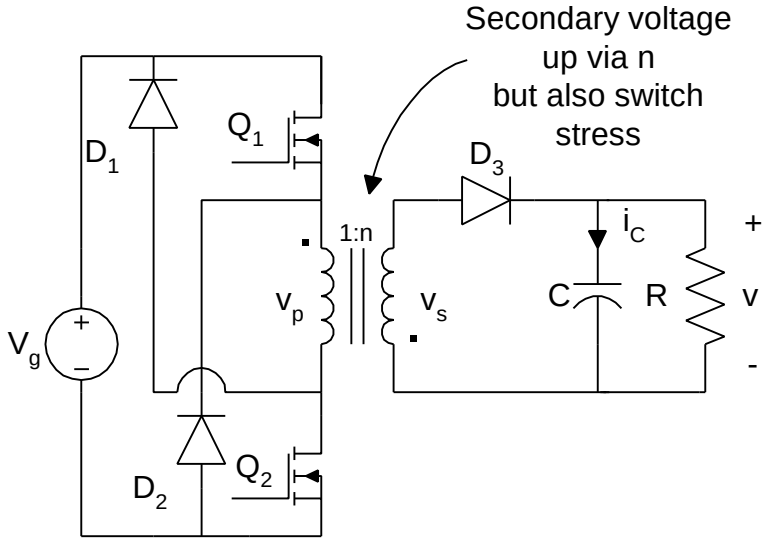
- I_{in} flows only during D_1T_s when Q_1 is turned on.
- I_{out} flows only during D_2T_s to charge the capacitor (flyback).
- But I_{out} (steady state) = V/R = I which always flows.

  Hence I_{in}(average) = $(n/D_2)I_{out}$. Higher secondary turns n

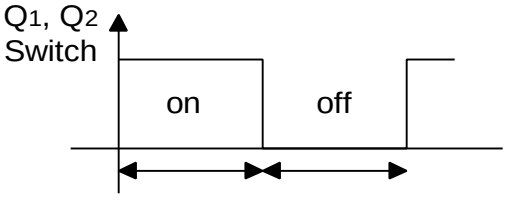
means higher I_{in}(average) is required in the primary.

C. Erickson Problem 6.4

We employ two Phase locked transistors to reduce stand-off voltage stress as shown below. This topology is an isolated version of the buck boost employing a transformer. The output voltage is boosted via the 1:n transformer but this also increases voltage switch stress on the diode, D_3. Q_1 and Q_2 have the same active control signal phasing to switch them both simultaneously. That is, both Q_1 and Q_2 are on during D_1 then both are off in the same direction during D_2.



Q_1 and Q_2 switch as follows even if DCM operation occurs because they are actively controlled.

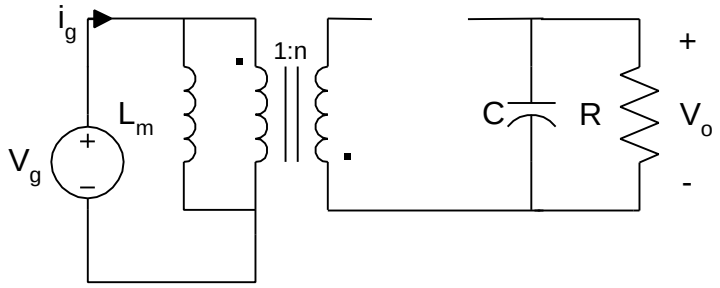


Under some load conditions diode #3 may turn off prematurely as shown below. We consider this case the DCM of operation and

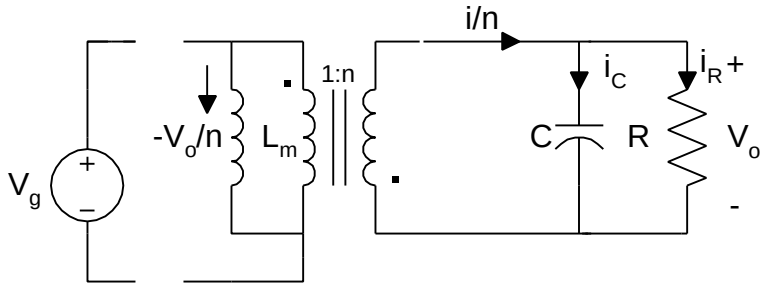
there will be three fractional time periods of the interval T_s: D_1, D_2 and D_3. Don't confuse fractional time duration's with diodes. Diodes "D_1" and "D_2" are off during interval D_1T_s when Q_1 and Q_2 transistors are on. IF during the interval D_2T_s, when the transistors are off, V_p tries to exceed V_g then diodes "D_1" and "D_2" will go on to clamp V_p to never exceed V_D. To start analysis assume Q_1 and Q_2 both go on at the same time and V_g is applied across the transformer primary but it takes time for i_{Lm} to build-up through the "L_m short" which temporarily violates Kirchoffs voltage law.

The DCM waveforms are in three time intervals and the circuits for the three intervals are shown on the next page:

<u>Period D_1T_s</u> Q_1 and Q_2 both on by control drive
D_3 is off due to reverse current flow from the dot convention

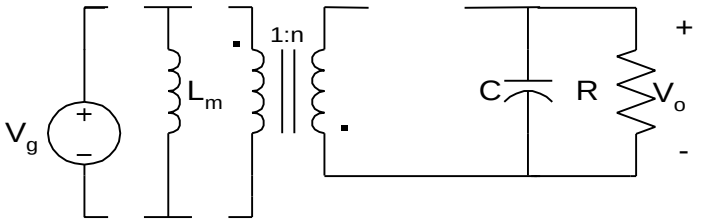


<u>Period D_2T_s</u> Q_1 and Q_2 both off by control drive and i(primary) loops flowing out of the dot.

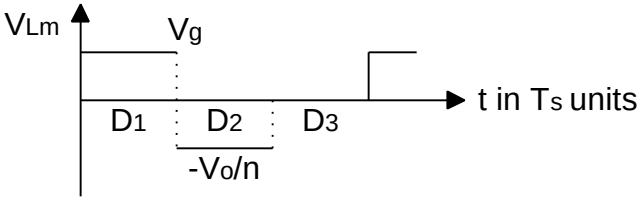


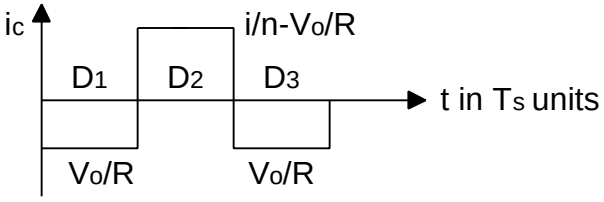
i(secondary) flows into the dot turning diode "D_3" on.
$V_g > V_o/n$ so that diodes "D_1" and "D_2" are both <u>off</u> (open).

<u>Period D_3T_s</u>: Q_1, Q_2 and diode "D_3"are <u>all</u> off



During the interval D_3T_s we consider that the secondary diode D_3 does not turn on and we have DCM in operation. Notice that i_c changes polarity when the secondary current is shut off.
From the three circuit diagrams we can plot V_L and i_c versus time in the three intervals D_1T_s, D_2T_s and D_3T_s.





$$< V_{Lm} >_{Ts} = 0 = D_1 V_g + D_2 \left(-\frac{V_o}{n}\right) + D_3 \text{ for steady state}$$

$$\frac{V_o}{V_g}\left(\begin{array}{c}\text{DCM}\\ \text{steady}\\ \text{state}\end{array}\right) = n\frac{D_1}{D_2}$$

n:1 transformer contribution

buck-boost DC gain (M(D) = D/D')

Again from the three circuit diagrams we can find the condition for the output capacitor $<i_c>_{Ts} = 0$ to achieve steady state. This will set the duration of D_1 via an upper limit condition.

$$D_1\left(-\frac{V_o}{R}\right) + D_2\left[\frac{i}{n} - \frac{V_o}{R}\right] + D_3\left(-\frac{V_o}{R}\right) = 0$$

$$D_2\, i/n = \frac{V_o}{R} \leftarrow (D_1+D_2+D_3)\, V_o/R = V_o/R$$

$$V_g\left[\frac{R\,T_s}{2L_m}\right] D_1 D_2 = V_o$$

$$\downarrow \qquad \downarrow$$

$$1/k \qquad \frac{nD_1}{V_o/V_g}$$

This sets the duration of the D_2T_s time interval, after which the DCM of operation begins.

$$\frac{1}{k}\, D^{2}{}_{1} = \left(\frac{V_o}{V_g}\right)^2 - \frac{V_o}{V_g} = \frac{D_1}{\sqrt{k}} = \frac{nD_1}{D_2} \Rightarrow D_2 = n\sqrt{k}$$

Since $V_g > \frac{V_o}{n}$, $\quad V_o < nV_g$, $\quad V_0 \equiv \frac{D_1 V_g}{\sqrt{k}}$

Hence, the duration of the first interval must be less than.

$$\Rightarrow D_1 < n\sqrt{K} = n\sqrt{\frac{2L_M}{R\,T_s}}$$

Finally, For HW#3 Due in 1 week:

1. Answer any questions asked throughout the lectures or in class
2. Chapter 6 Problems 7, 8, and 11.

Some hints on problem 11 will be given today time permitting.

III. Flyback Converter Mode Transformer

In the flyback transformer the primary winding conducts storing energy in the core air gap, but, the secondary winding does not conduct while the primary conducts. Then the secondary winding conducts removing the energy stored in the air gap, but, the primary winding does not conduct while the secondary does. Therefore traditional transformer relationships reflecting impedances via the turns ratios do not apply.

The key parameter is the expected PEAK CURRENT. As the primary winding acts as an inductor rather than a transformer we find:

$$I_{peak} = \frac{V_{in}(min)\, T_{on}}{L_{primary}} \qquad \text{where } T_{on} = D_{max} \times T_{sw}$$

Where D_{max} is the maximum duty cycle expected and $V_{in}(min)$ is the minimum input Dc voltage expected. To insure that we do not exceed I_{peak} we have to choose a sufficiently large inductor value.

$$L_{primary} = \frac{V_{in}(min) \times D_{max} \times T_{sw}}{I_{peak}}$$

The energy stored in the core during each on time is:

$$E(\text{stored in the air gap}) = \tfrac{1}{2} \times L_{primary} \times I(peak)^2$$

On a steady-state basis we have a power out that must be fed by the energy I the air gap. That is:

$$P(\text{air gap}) = 1/2 \times E(\text{air gap}) \times f_{sw}$$

Now the voltage equations for the two sets of turns are modified from the usual transformer equations as follows:

$$\frac{V_{sec}\,(1-D)}{N_{sec}} = \frac{V_{prim} \times D}{N_{prim}}$$

Hence to a first approximation we can estimate the required

number of secondary turns as:

$$N_{secondary} = \frac{N_{prim} \times V_{out} \times (1-D_{max})}{V_{in}(min) \times D_{max}}$$

This is the maximum number of turns we need to employ. Clearly, we have to round off to the nearest integer value for the number of turns.

A crude estimate of the minimum switch requirements can be taken from the following table:

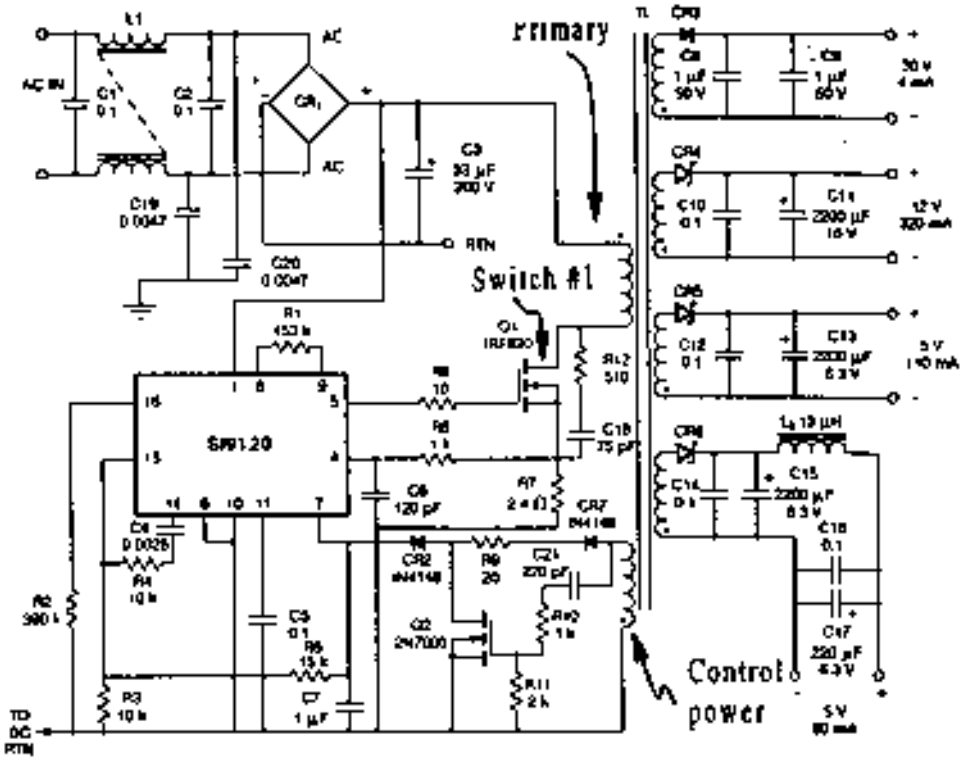
Estimating the Significant Minimum Parameters of the Power Semiconductors

	Bipolar Power Switch		MOSFET Power Switch		Rectifier(s)	
Topology	V_{CEO}	I_C	V_{DSS}	I_D	V_R	I_F
Flyback	$1.7V_{in(max)}$	$\frac{2P_{out}}{V_{in(min)}}$	$1.5V_{in(max)}$	$\frac{2P_{out}}{V_{in(min)}}$	$10V_{out}$	I_{out}

A full blown flyback converter schematic is given on the following page

Find on this schematic the following:

- the input mains/EMI filter
- the four isolated outputs
- the primary winding and the PWM switch
- the control chip power circuits
- the controller chip and ancillary circuits



Commercial 5 W flyback converter for 170 V input and multiple outputs. From C. Varga, *Application Note AN90-2*. Santa Clara: Siliconix. 1990. Reprinted by permission.